
Signal Integrity Report

FX10 Mezzanine Connector (5mm w/o ground plate)

Version 1.0

September 12, 2009

09HSI-S030-R1-CHA



HIROSE ELECTRIC (U.S.A.), INC.
20400 STEVENS CREEK BLVD., SUITE 250
SAN JOSE, CA 95014
PHONE: 408-253-9640, FAX: 408-253-9641

Table of Contents

Table of Contents	ii
1. Introduction.....	4
2. Geometry	4
3. Differential Signals	4
3.1 Frequency-Domain Modeling.....	4
3.1.1 S parameters (connector only).....	4
3.1.2 W-element Model (PCB trace).....	9
3.2 Time-Domain Simulation	11
3.2.1 Impedance Profile (connector only).....	11
3.2.2 TDR and TDT waveforms (connector only).....	12
3.2.3 Time-Domain Crosstalk (connector only).....	14
3.2.4 System Voltage and Timing Margins.....	14
4. Single-ended Signals	20
4.1 Frequency-Domain Modeling.....	20
4.1.1 S parameters (connector only).....	20
4.1.2 W-element Model (PCB trace).....	22
4.2 Time-Domain Simulation	23
4.2.1 Impedance Profile (connector only).....	23
4.2.2 TDR and TDT waveforms (connector only).....	24
4.2.3 Time-Domain Crosstalk (connector only).....	25
4.2.4 System Voltage and Timing Margins.....	26
5. Measurement.....	29
5.1 Measurement Setup	29
5.2 Differential Signals.....	30
5.2.1 Measurement vs. Simulation Correlation (connector only)	30
5.2.2 Time-Domain NEXT and FEXT.....	32
5.2.3 Impedance profile.....	33
5.3 Single-ended Signals	33
5.3.1 Measurement vs. Simulation Correlation (connector only)	33
5.3.2 Time-Domain NEXT and FEXT.....	35
5.3.3 Impedance profile.....	35
6. Appendix.....	37

Revision History

Name	Date	Reason For Changes	Version
Fernando Cheng	09-21-09	First created	1.0

1. Introduction

The FX10 series is an SMT board-to-board connector that works up to 15+Gbps for portable electronics applications. It features reinforced fittings which provide greater adhesion to the board and protect against solder peeling. The signal contact pitch of 0.5mm results in a smaller connector footprint for high-density PCB mounting.

In the following sections, we will describe the FX10 geometry and the signal integrity analysis results for the 5mm stack height with no ground plate. The signal integrity results include the S parameters, TDR and TDT waveforms, and eye diagrams.

The FX10-5mm-noGND connector complies with the IEEE 802.3ap spec for return loss (RL) and insertion-loss-to-crosstalk-ratio (ICR) to 15+Gbps, and introduces small timing jitter end eye height degradation.

2. Geometry

Figure 1 shows the structure of FX10 connector, which consists of a header and a receptacle. The total stack height is flexible. For example, the following heights are made available: 4mm and 5mm.

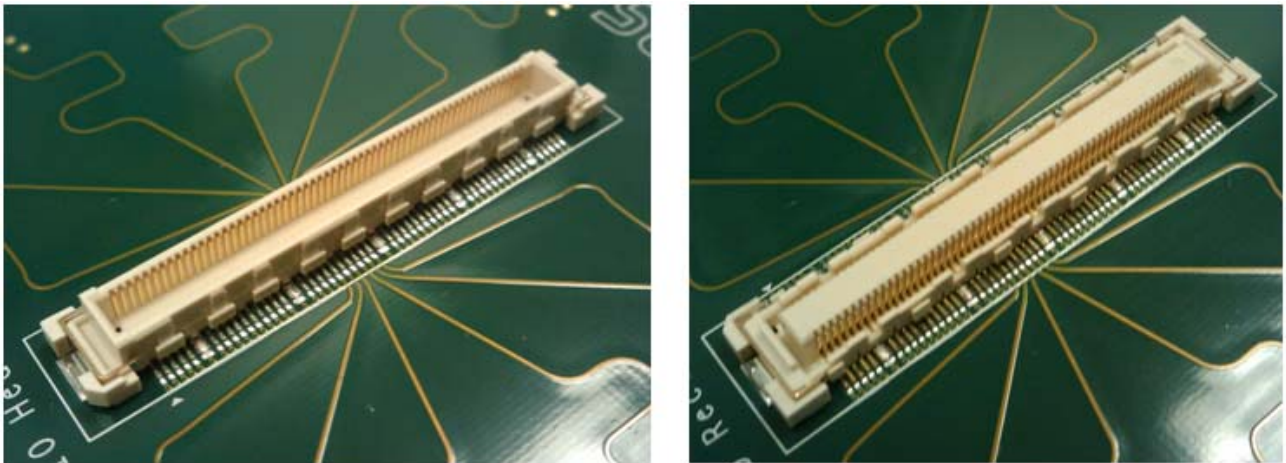


Figure 1 FX10 connector

3. Differential Signals

3.1 Frequency-Domain Modeling

3.1.1 S parameters (connector only)

Figure 2 shows the simulation model for FX10-5mm-noGND (connector only). We used symmetry to combine four quarter models created from HFSS into a 40-port single ended Touchstone file first. Then, the four outermost pins are pre-assigned as ground, resulting in a 32-port Touchstone file. Additional pins can be assigned as ground, depending on the pin assignment.

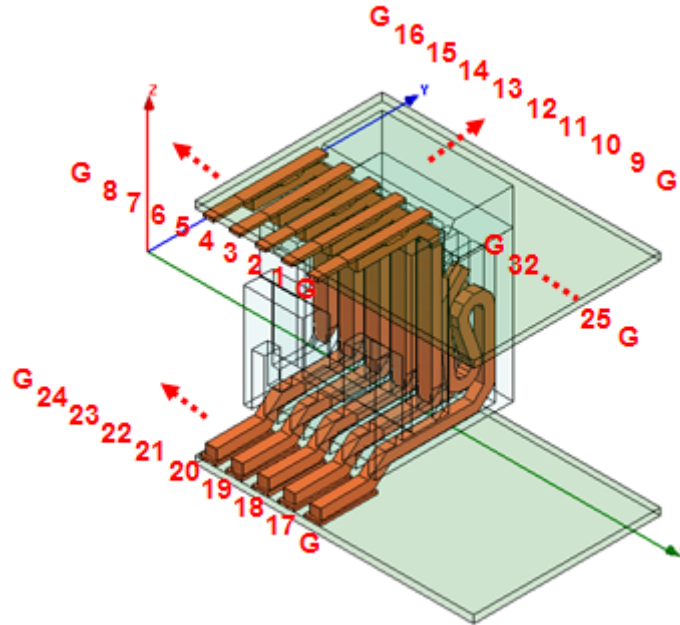


Figure 2 FX10-5mm-noGND simulation model

The GSGSG pin assignment configuration, as shown in Figure 3, is recommended for the FX10-5mm-noGND connector. Ports 1 and 3 are grouped into Pair 1, and Ports 5 and 7 are grouped into Pair 2, etc. Figure 4 shows the corresponding SDD for pair 3 (or Ports 10 and 12), where the insertion loss (IL), return loss (RL), and crosstalk can be clearly seen, and are summarized in Table 1.

The impedance and trace delay values for each of the 4 differential pairs are shown in Table 2.

Figure 5 shows the return loss (RL) comparison with the IEEE802.3ap spec for pair 3. Figure 6 - Figure 9 show the power sum and insertion-to-crosstalk ratio (ICR) profile comparison with the IEEE802.3ap spec of NEXT and FEXT respectively. For the power sum and ICR plots, we combine the crosstalk effects from the five neighboring pairs of pair 3 (we consider additional crosstalk effects of pair 4 to pair 3, and pair 4 to pair 1 to represent pairs to the left of pair 3, not shown in the picture).

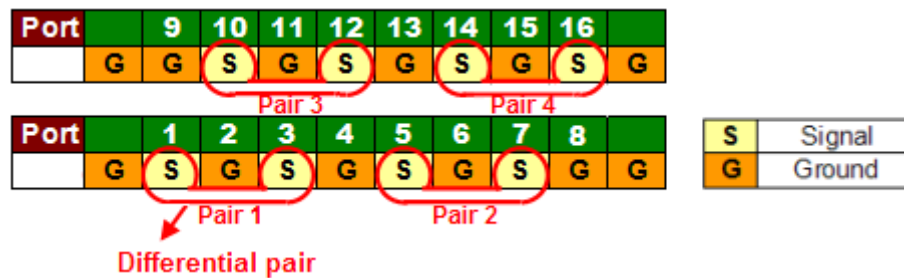


Figure 3 FX10-5mm-noGND pin assignment

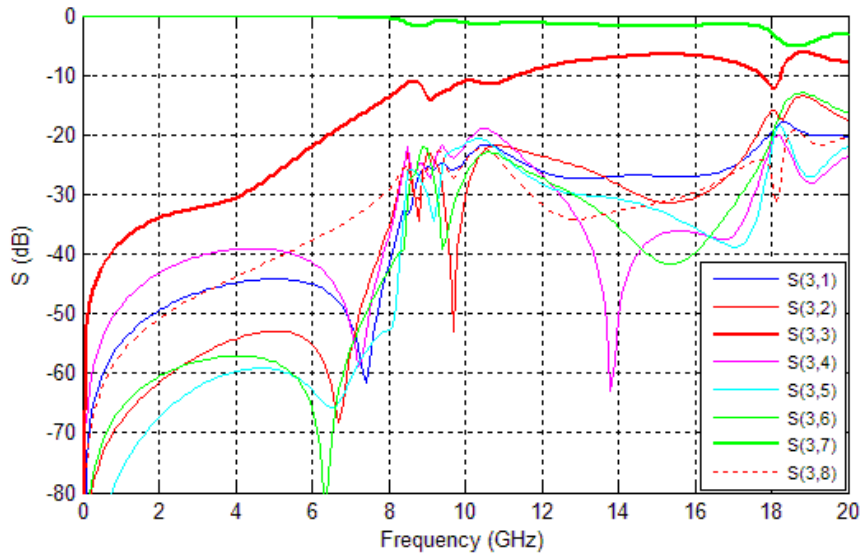


Figure 4 SDD for pair 3 (ports 10-12) of FX10-5mm-noGND

FREQUENCY (GHZ)	INSERTION LOSS (DB)	RETURN LOSS (DB)	WORST PAIR-TO-PAIR NEXT (DB)	WORST PAIR-TO-PAIR FEXT (DB)
2.5	-0.097	-33.02	-41.62	-48.78
3.125	-0.115	-32.18	-40.25	-46.59
4	-0.140	-30.54	-39.22	-43.87
5	-0.172	-26.66	-39.30	-40.88
6.25	-0.233	-20.82	-42.61	-36.89
8	-0.517	-13.69	-35.28	-29.14

Table 1 Summary of SDD for pair 3 (ports 10-12) of FX10-5mm-noGND

		FX10-5mm no GND Differential Impedance (Ohm)				FX10-5mm no GND Differential Delay (ps)	
Row	2	Pair 3 104.16	Pair 4 104.30	Row	2	Pair 3 55.78	Pair 4 55.81
	1	Pair 1 104.30	Pair 2 104.16		1	Pair 1 55.81	Pair 2 55.78

Table 2 Summary of connector's differential impedance and delay at 0.5 GHz

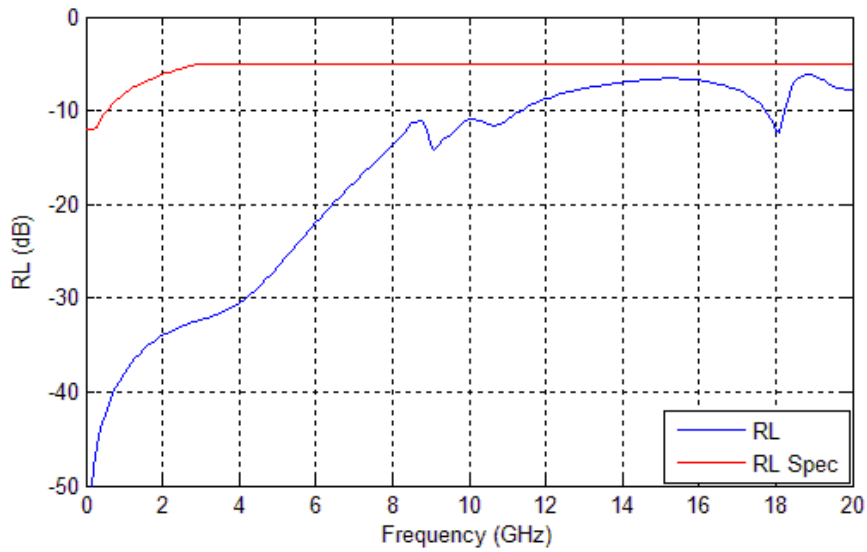


Figure 5 RL profile for pair 3 of connector only

The RL profile for the center pair of the FX10-5mm-noGND connector meets the IEEE 802.3ap spec up to 20+GHz. Half wavelength resonances occur at 9 GHz and 18 GHz as individual ground traces are tied together only at the entrance and exit of the connector.

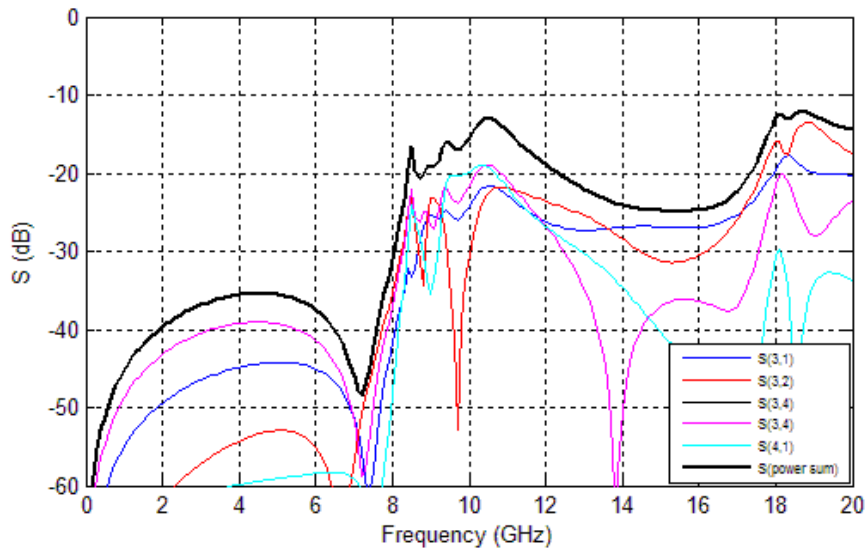


Figure 6 Power Sum of NEXT for pair 3 of connector only

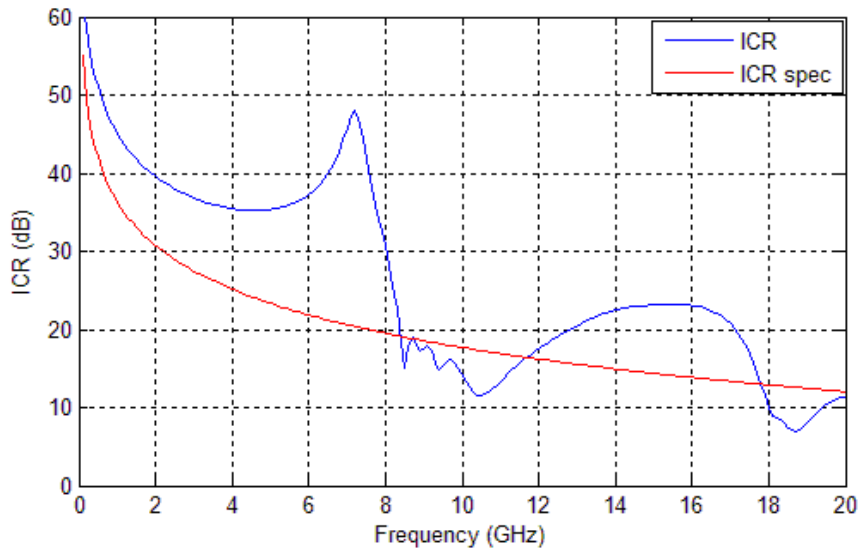


Figure 7 ICR profile of NEXT for pair 3 of connector only

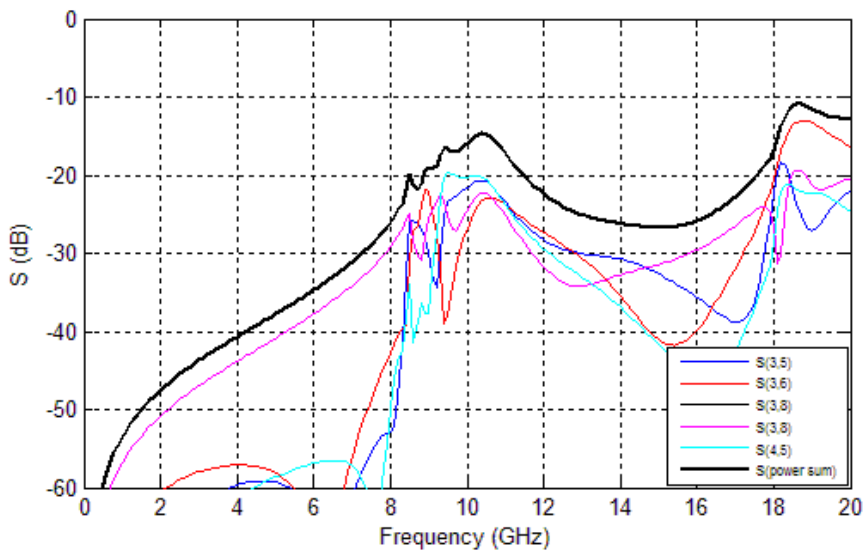


Figure 8 Power Sum of FEXT for pair 3 of connector only

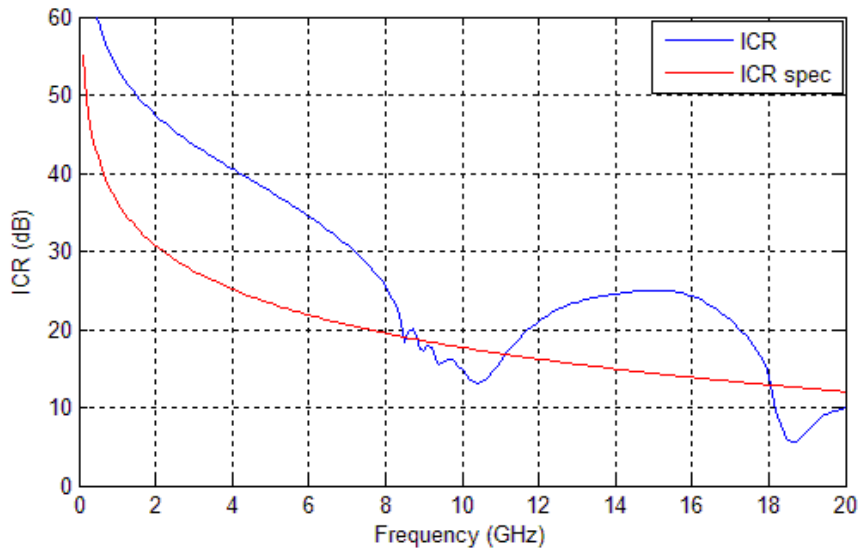


Figure 9 ICR profile of FEXT for pair 3 of connector only

The ICR profile for FEXT and NEXT satisfies the IEEE 802.3ap spec up to 8 GHz.

3.1.2 W-element Model (PCB trace)

An example of signal traces in the PCB uses the microstrip cross section in Figure 10 for 100 Ohms differential impedance. The corresponding W-element model and differential S parameters are shown in Figure 11 and Figure 12.

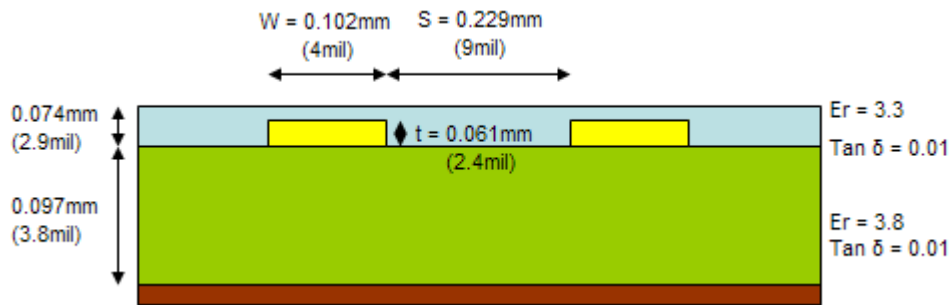


Figure 10 Cross section of PCB traces

```

* No. of lines
2

* Lo
3.327267e-007
4.557374e-008 3.327267e-007

* Co
1.053540e-010
-9.192936e-012 1.053540e-010

* Ro
0.000000e+000
0.000000e+000 0.000000e+000

* Go
0.000000e+000
0.000000e+000 0.000000e+000

* Rs
1.445199e-003
1.958840e-004 1.445199e-003

* Gd
6.112824e-012
-4.019081e-013 6.112824e-012
    
```

Figure 11 W-element models (in per meter) of Figure 10

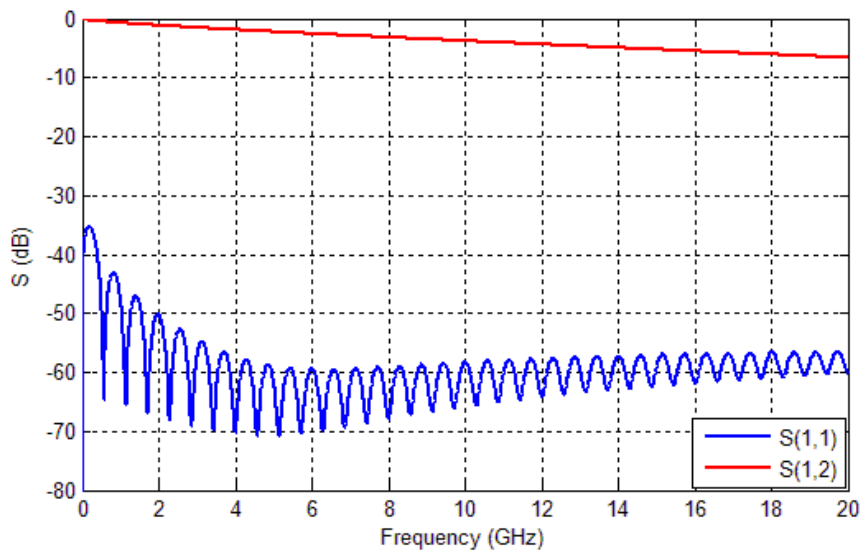


Figure 12 Differential S parameters (SDD) of 6" PCB traces

3.2 Time-Domain Simulation

3.2.1 Impedance Profile (connector only)

The impedance profiles for pair 3 of the FX10-5mm-noGND connector at 30ps, 60ps and 120ps rise time and 20GHz bandwidth are shown in Figure 13, Figure 14 and Figure 15.

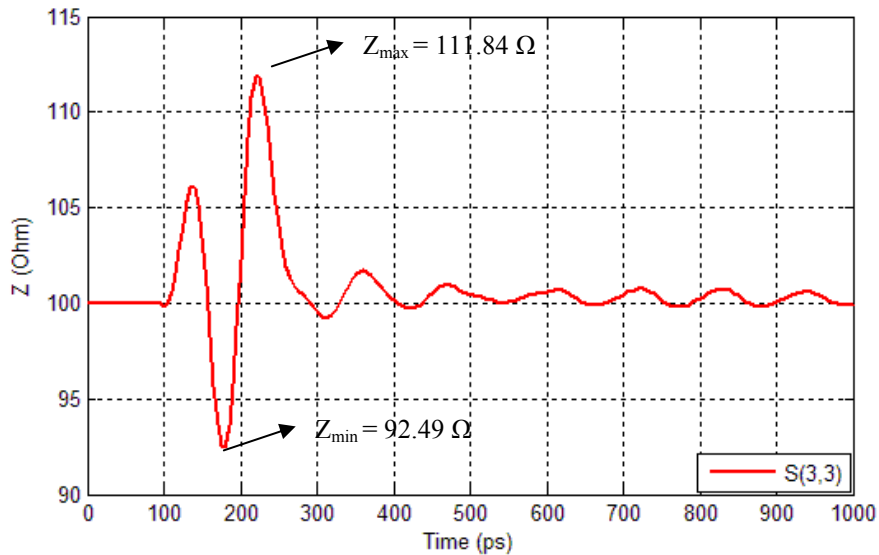


Figure 13 Impedance profile for pair 3 of FX10-5mm-noGND @30ps rise time (20% to 80%) and 20GHz BW

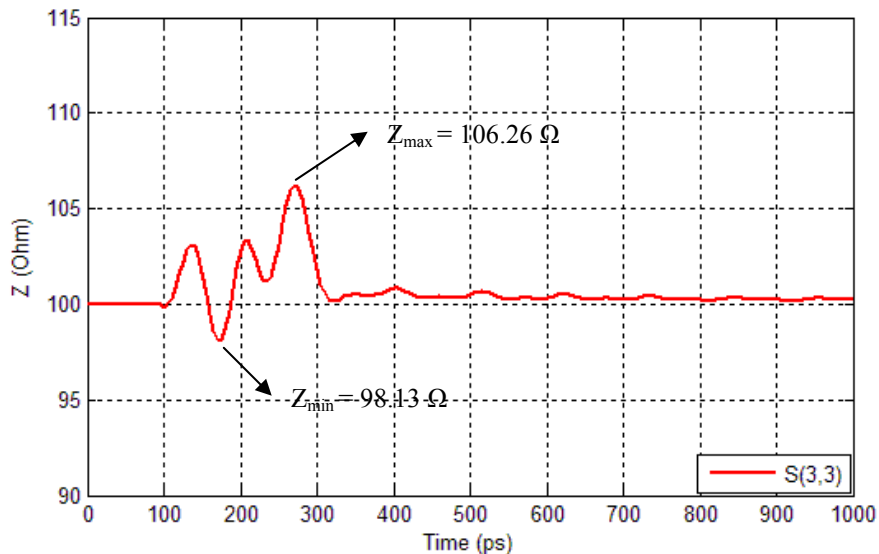


Figure 14 Impedance profile for pair 3 of FX10-5mm-noGND @60ps rise time (20% to 80%) and 20GHz BW

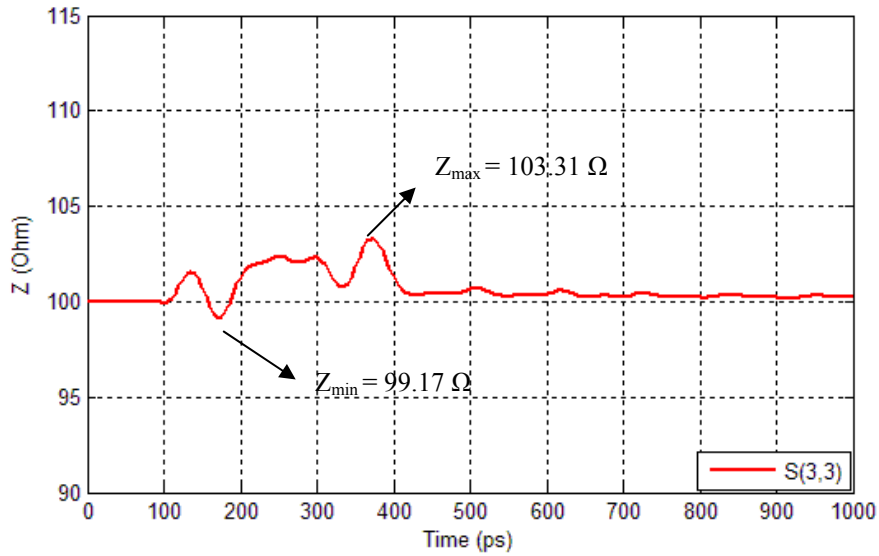


Figure 15 Impedance profile for pair 3 of FX10-5mm-noGND @120ps rise time (20% to 80%) and 20GHz BW

3.2.2 TDR and TDT waveforms (connector only)

Figure 16 - Figure 18 show the TDR and TDT waveforms at 30ps, 60ps and 120ps rise times (20% to 80%) for pair 3 of the FX10-5mm-noGND connector. The worst crosstalk values to the center pair are summarized in Table 3.

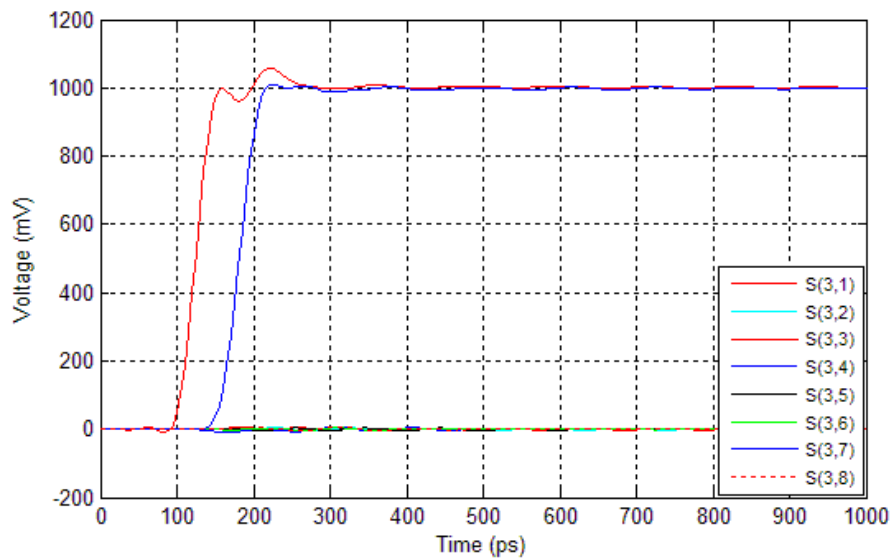


Figure 16 TDR and TDT waveforms @30ps rise time (20% to 80%) and 20GHz BW for pair 3 of FX10-5mm-noGND

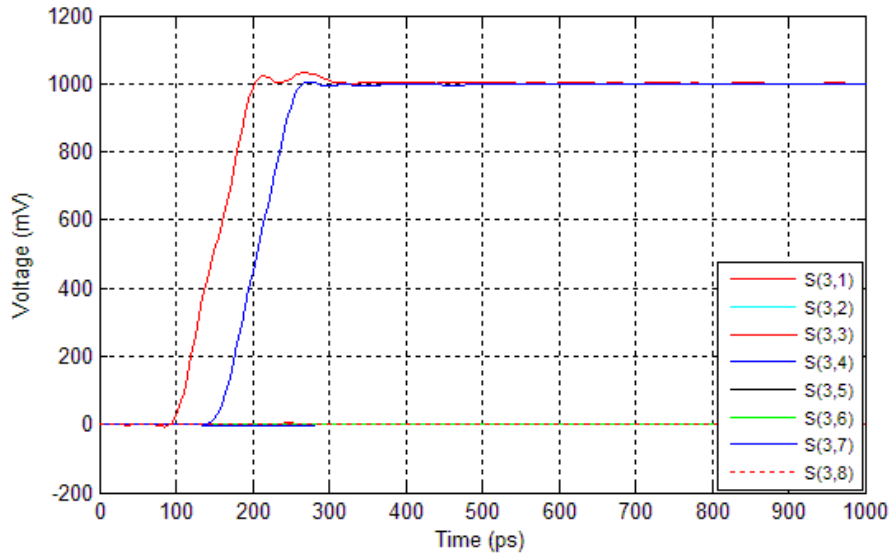


Figure 17 TDR and TDT waveforms @60ps rise time (20% to 80%) and 20GHz_z BW for pair 3 of FX10-5mm-noGND

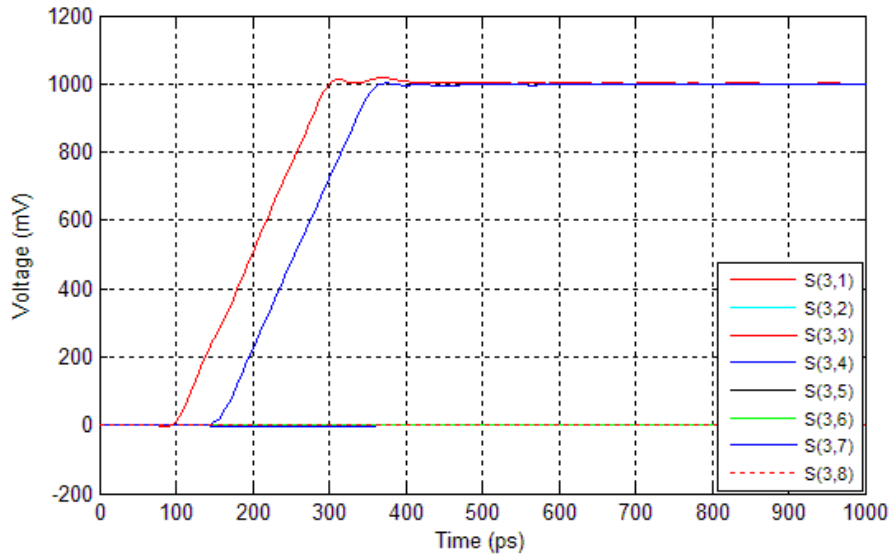


Figure 18 TDR and TDT waveforms @120ps rise time (20% to 80%) and 20GHz_z BW for pair 3 of FX10-5mm-noGND

20% TO 80% RISE TIME (PS)	WORST PAIR-TO-PAIR NEXT (%)	WORST PAIR-TO-PAIR NEXT (%)
30	0.862	0.628
60	0.456	0.326
120	0.386	0.166

Table 3 Summary of Time-domain SDD @ 20GHz_z BW for pair 3 of FX10-5mm-noGND

3.2.3 Time-Domain Crosstalk (connector only)

The total differential crosstalk values in % for 60ps (20% to 80%) rise time and 20GHz bandwidth for pair 3 of the FX10 connector is shown in Figure 19.

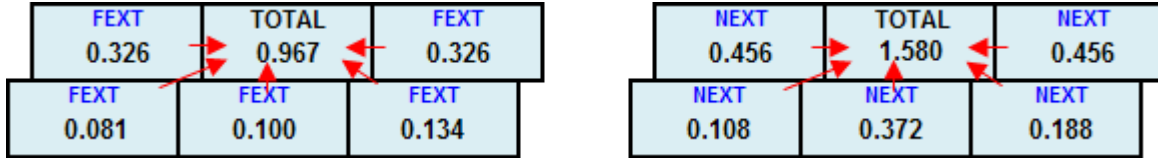


Figure 19 Differential crosstalk (in %) from simulations for pair 3 using step input with 60ps (20% to 80%) rise time and 20GHz BW

3.2.4 System Voltage and Timing Margins

To demonstrate the FX10’s performance, we ran simulations with the following setup:

- Ideal voltage source
- Center pair of the FX10 connector
- 152.4mm (6 inches) PCB trace from driver to FX10 connector, and 152.4mm (6 inches) PCB trace from FX10 connector to receiver

Note: Since the time steps used for the simulations were of 1ps, the timing jitter values have an error margin of 1ps. The eye height is defined as the absolute maximum eye opening.

Table 4 and Table 5 show the optimized tap coefficients for the maximum eye opening at various data rates for the channel without the connector (base case) and for the full channel with connector. The base case does not include crosstalk effects. The full FX10 channel model (with connector) and base case (without connector) are depicted in Figure 20.

Figure 21 - Figure 26 show the eye diagrams at receiver inputs for various data rates (5, 6.25, 8, 10, 12.5 and 16Gbps) with 5 FEXT. Table 6 summarizes the corresponding results for the eye diagram and their comparison with the base case.

Column ΔFX10 is the timing jitter or voltage loss caused by the FX10 connector.

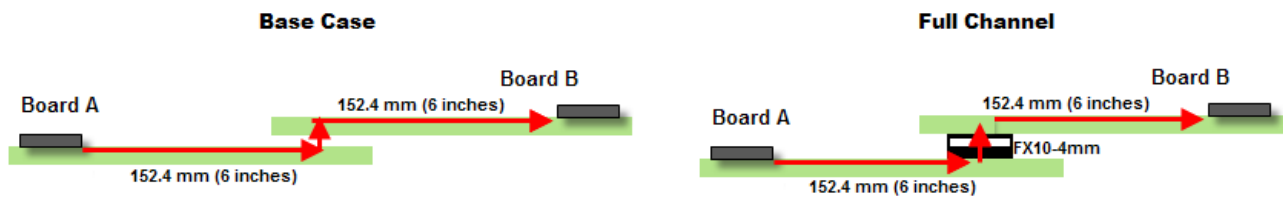


Figure 20 Channel models used for eye diagram simulations

Data Rate (Gbps)	PRE-CURSOR[1]	MAIN CURSOR	POST-CURSOR[1]
5	----	0.9284	-0.0716
6.25	-0.0280	0.8936	-0.0784
8	-0.0348	0.8720	-0.0932
10	-0.0457	0.8479	-0.1065
12.5	-0.0599	0.8189	-0.1213
16	-0.0780	0.7825	-0.1395

Table 4 Base case: optimum tap setting coefficients for pair 3 of FX10-5mm-noGND connector

Data Rate (Gbps)	PRE-CURSOR[1]	MAIN CURSOR	POST-CURSOR[1]
5	----	0.9257	-0.0743
6.25	-0.0262	0.8902	-0.0836
8	-0.0348	0.8686	-0.0965
10	-0.0497	0.8458	-0.1044
12.5	-0.0664	0.8135	-0.1200
16	-0.0915	0.7638	-0.1447

Table 5 Full channel: optimum tap setting coefficients for pair 3 of FX10-5mm-noGND connector

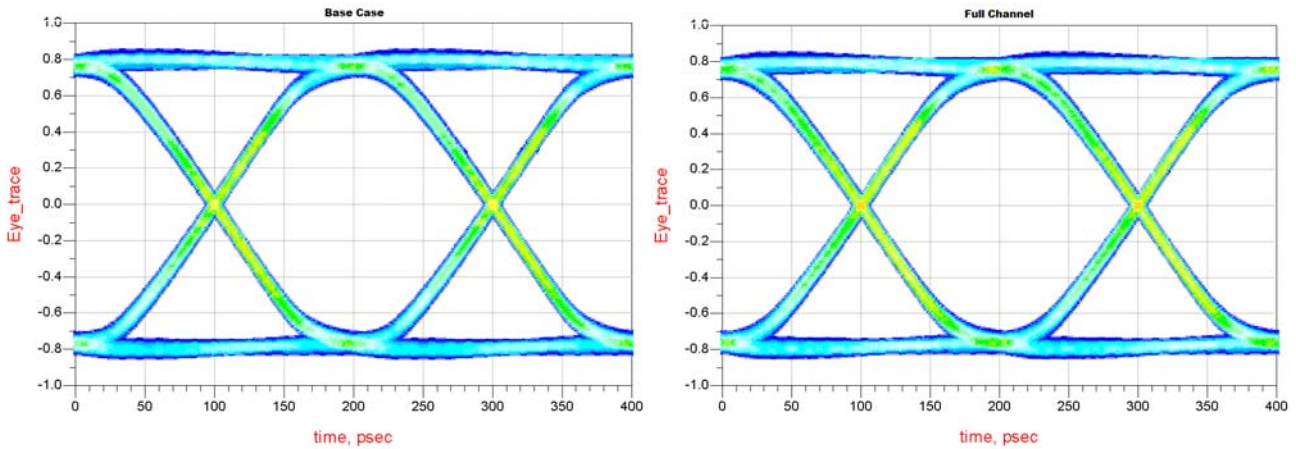


Figure 21 Base case and full channel eye diagram at receiver input for 5Gbps data rate 5 FEXT

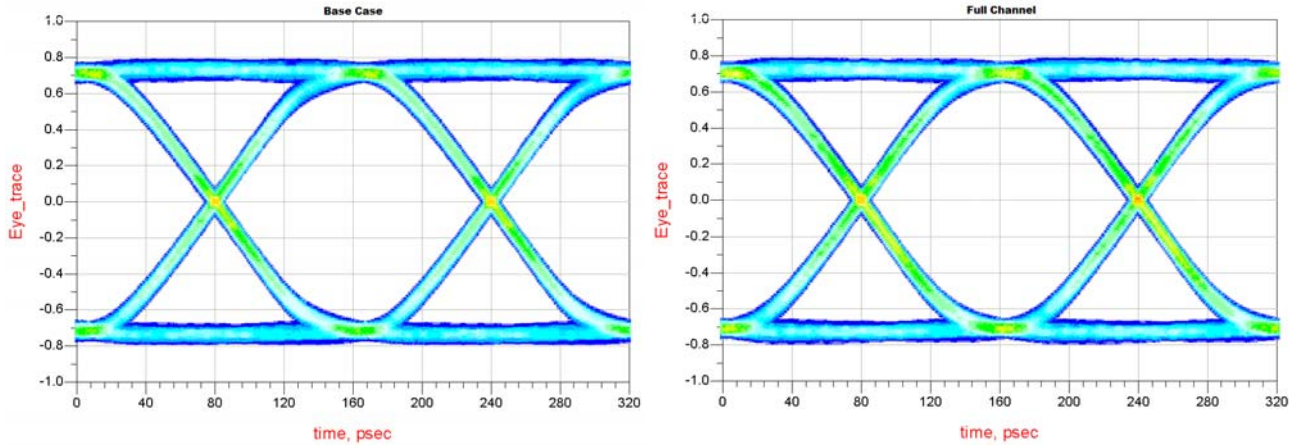


Figure 22 Base case and full channel eye diagram at receiver input for 6.25Gbps data rate 5 FEXT

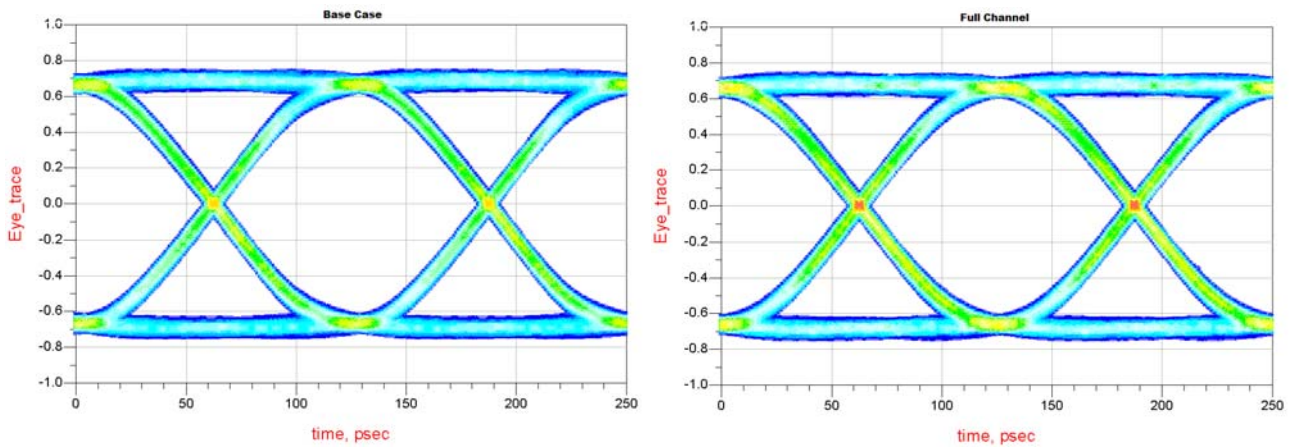


Figure 23 Base case and full channel eye diagram at receiver input for 8Gbps data rate 5 FEXT

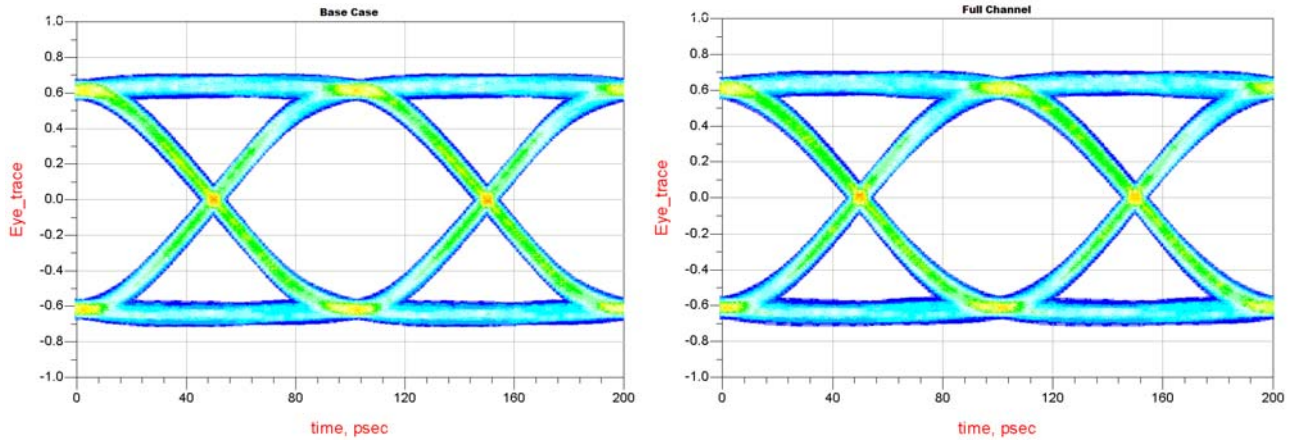


Figure 24 Base case and full channel eye diagram at receiver input for 10Gbps data rate 5 FEXT

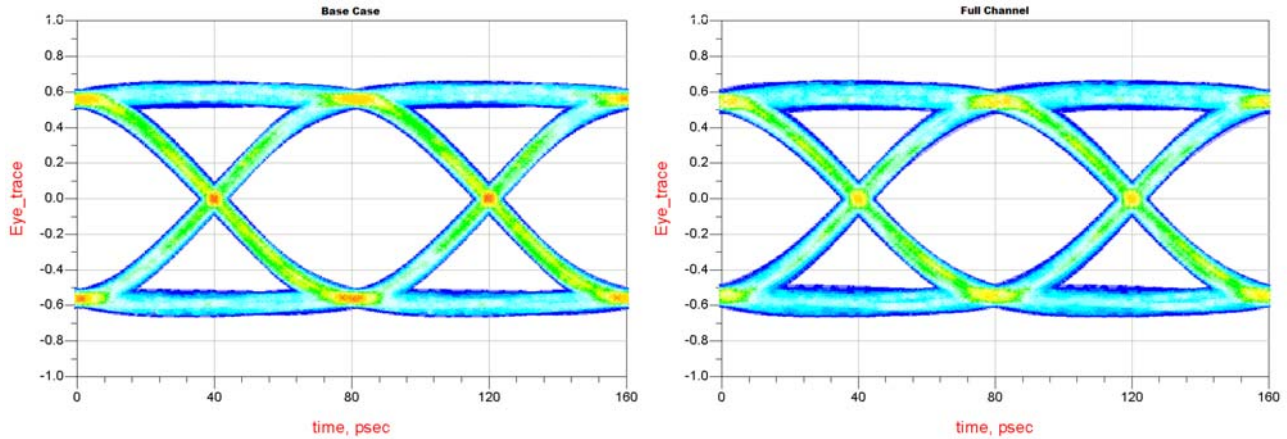


Figure 25 Base case and full channel eye diagram at receiver input for 12.5Gbps data rate 5 FEXT

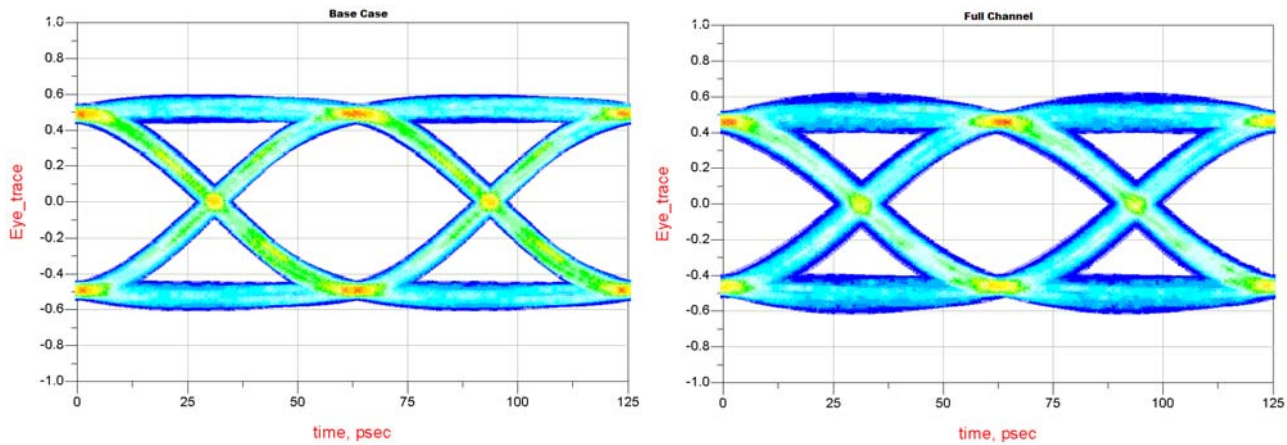


Figure 26 Base case and full channel eye diagram at receiver input for 16Gbps data rate 5 FEXT

Data Rate (Gbps)	Timing Jitter (ps)				Eye Height (mV)			
	FX10	Base Case	Δ FX10	Δ FX10 (%)	FX10	Base Case	Δ FX10	Δ FX10 (%)
5	6.41	6.52	-0.11	-0.05	1424.21	1437.67	-13.46	-0.94
6.25	7.03	6.56	0.47	0.29	1332.09	1352.52	-20.43	-1.51
8	6.96	6.45	0.51	0.41	1236.17	1255.15	-18.98	-1.51
10	6.53	6.61	-0.08	-0.08	1131.31	1150.31	-19.00	-1.65
12.5	6.93	6.19	0.74	0.92	977.99	1033.79	-55.80	-5.40
16	9.78	6.05	3.73	5.97	819.31	903.73	-84.42	-9.34

Table 6 Comparison of eye height and timing jitter between full channel and Base Case at the receiver's input with 5 FEXT

Figure 27 - Figure 32 show the eye diagrams at receiver inputs for various data rates (5, 6.25, 8, 10, 12.5 and 16Gbps) with 5 NEXE. Table 7 summarizes the corresponding results for the eye diagram and their comparison with the base case.

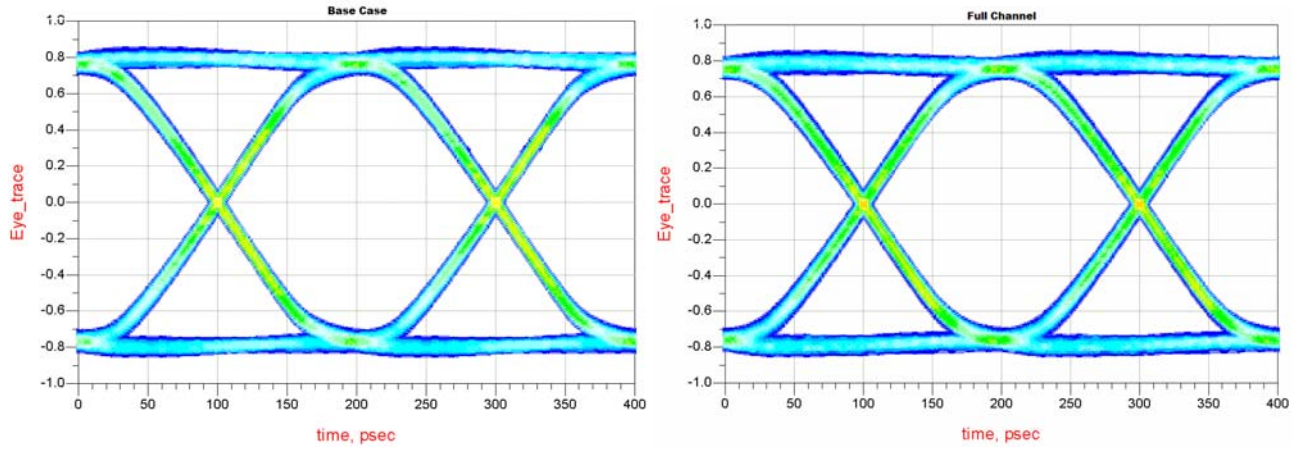


Figure 27 Base case and full channel eye diagram at receiver input for 5Gbps data rate 5 NEXT

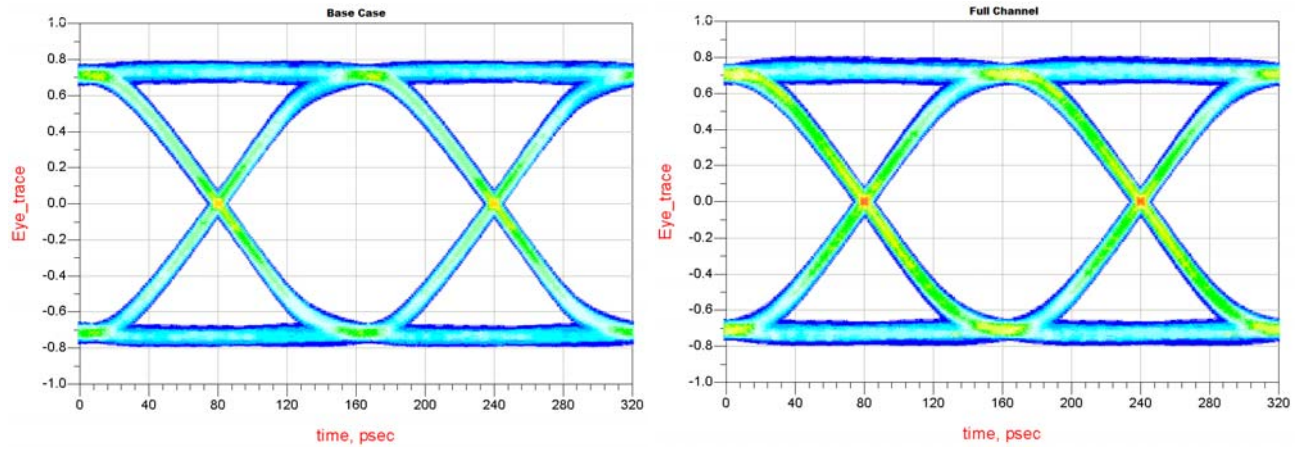


Figure 28 Base case and full channel eye diagram at receiver input for 6.25Gbps data rate 5 NEXT

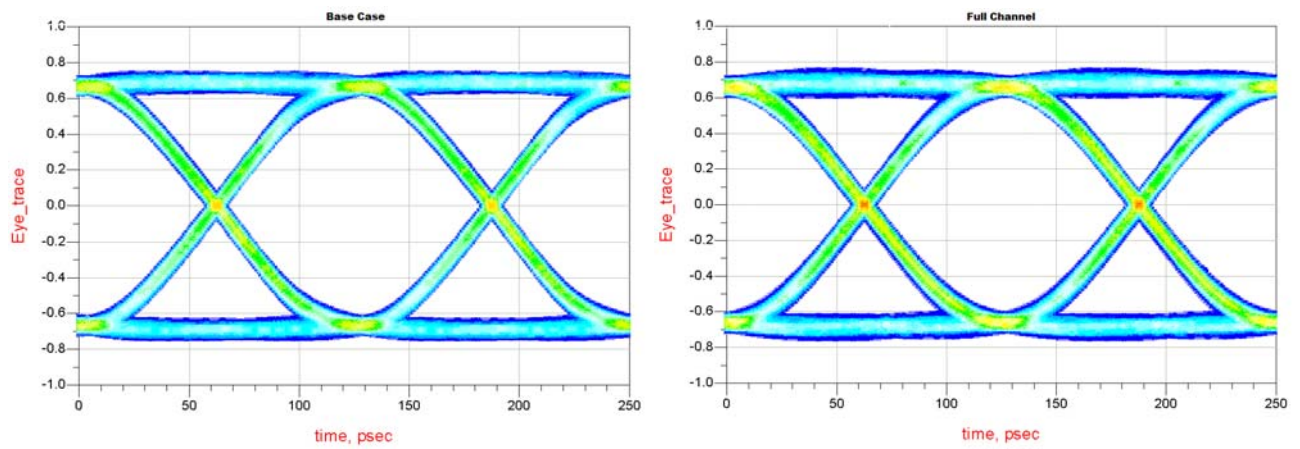


Figure 29 Base case and full channel eye diagram at receiver input for 8Gbps data rate 5 NEXT

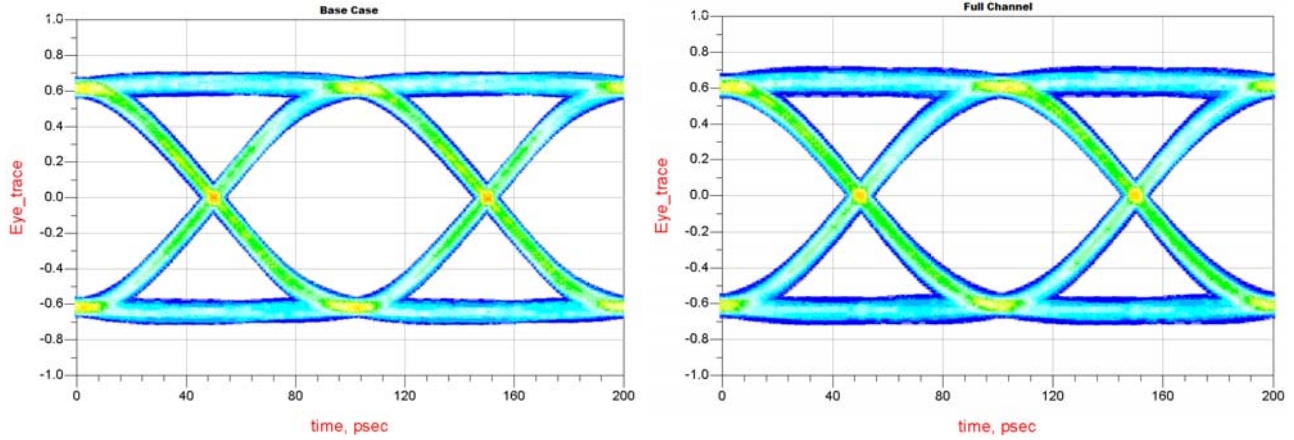


Figure 30 Base case and full channel eye diagram at receiver input for 10Gbps data rate 5 NEXT

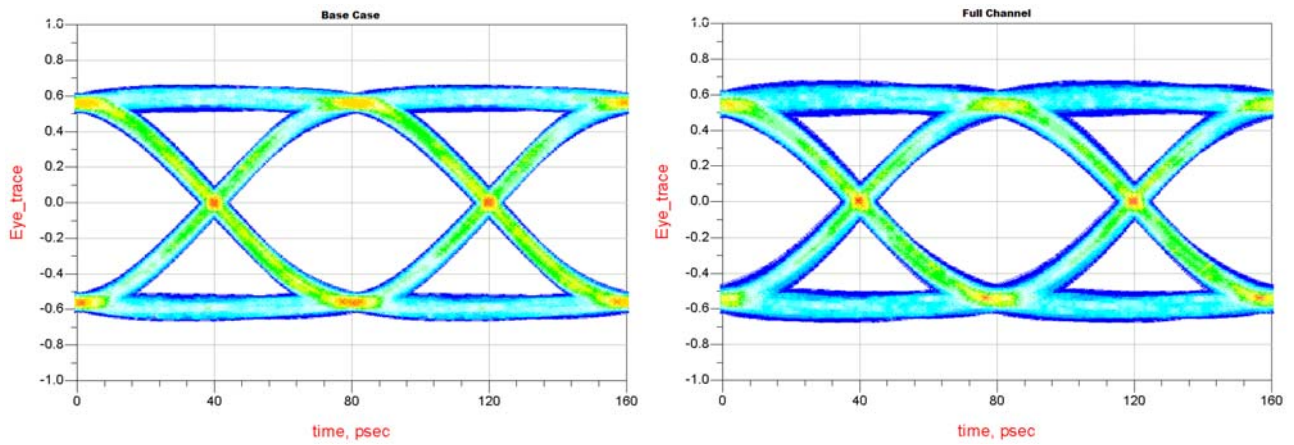


Figure 31 Base case and full channel eye diagram at receiver input for 12.5Gbps data rate 5 NEXT

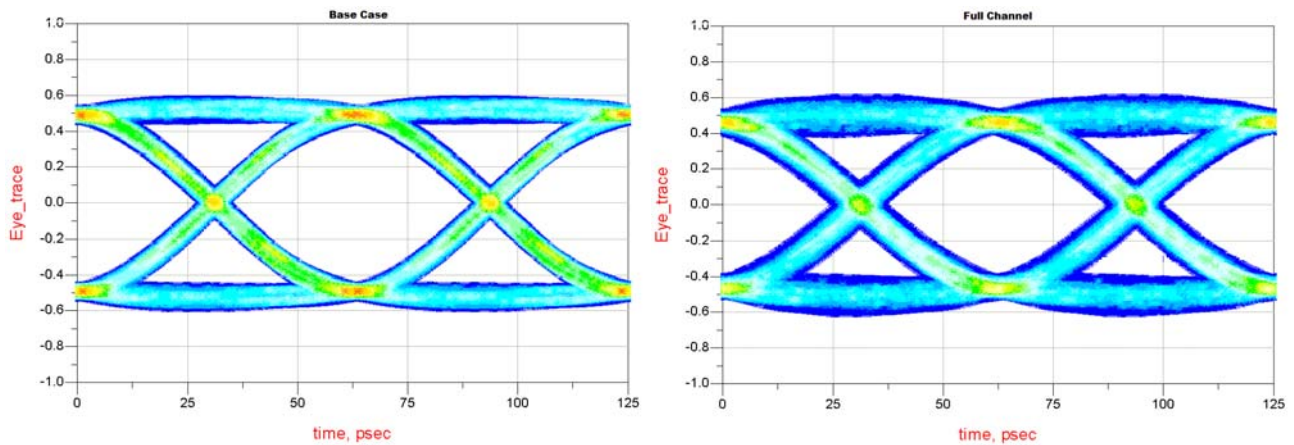


Figure 32 Base case and full channel eye diagram at receiver input for 16Gbps data rate 5 NEXT

Data Rate (Gbps)	Timing Jitter (ps)				Eye Height (mV)			
	FX10	Base Case	Δ FX10	Δ FX10 (%)	FX10	Base Case	Δ FX10	Δ FX10 (%)
5	8.46	6.52	1.94	0.97	1420.88	1437.67	-16.79	-1.17
6.25	7.40	6.56	0.84	0.52	1326.66	1352.52	-25.86	-1.91
8	7.56	6.45	1.11	0.89	1229.60	1255.15	-25.55	-2.04
10	6.84	6.61	0.23	0.23	1110.42	1150.31	-39.89	-3.47
12.5	8.04	6.19	1.85	2.31	952.52	1033.79	-81.27	-7.86
16	10.74	6.05	4.69	7.50	810.42	903.73	-93.31	-10.32

Table 7 Comparison of eye height and timing jitter between full channel and Base Case at the receiver's input with 5 NEXT

4. Single-ended Signals

4.1 Frequency-Domain Modeling

4.1.1 S parameters (connector only)

A 32-port single-ended Touchstone file was used as described in Section 3.1.1. The single-ended pin assignment is shown in Figure 33. Figure 34 shows the corresponding S-parameters for port 13, where the insertion loss (IL), return loss (RL), and crosstalk can be clearly seen, and are summarized in Table 8.

Impedance and trace delay values for each of the 8 single-ended pins are shown in Table 9.

Figure 35 and Figure 36 show the absolute sum of near-end and far-end crosstalk, respectively.

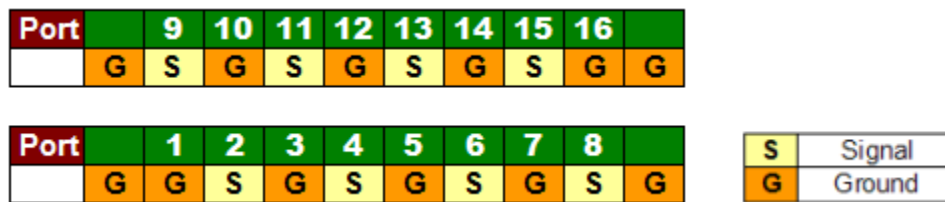


Figure 33 FX10-5mm-noGND single-ended pin assignment

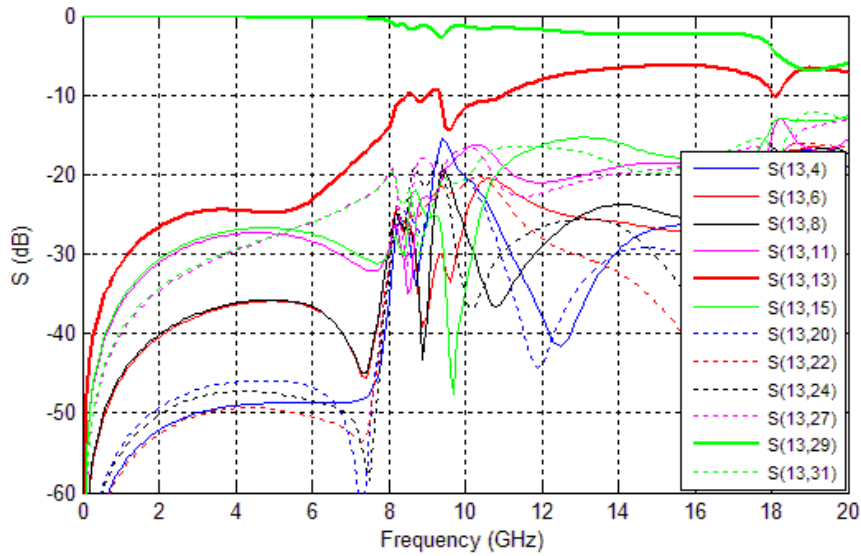


Figure 34 S-parameters for port 13 of connector only

FREQUENCY (MHZ)	INSERTION LOSS (DB)	RETURN LOSS (DB)	WORST PAIR-TO-PAIR NEXT (DB)	WORST PAIR-TO-PAIR FEXT (DB)
400	-0.032	-38.02	-43.64	-47.31
533	-0.038	-35.89	-41.23	-44.94
800	-0.051	-32.87	-37.87	-41.60

Table 8 Summary of S-parameters for port 13 of connector only

		FX10-5mm no GND Single-ended Impedance (Ohm)						FX10-5mm no GND Single-ended Delay (ps)			
Row	2	Port 9	Port 11	Port 13	Port 15	Row	2	Port 9	Port 11	Port 13	Port 15
		54.63	54.21	54.36	54.66			57.39	57.04	57.02	57.50
	1	Port 2	Port 4	Port 6	Port 8		1	Port 2	Port 4	Port 6	Port 8
		54.66	54.36	54.21	54.63			57.50	57.02	57.04	57.39

Table 9 Summary of connector's single-ended impedance and delay at 0.5 GHz

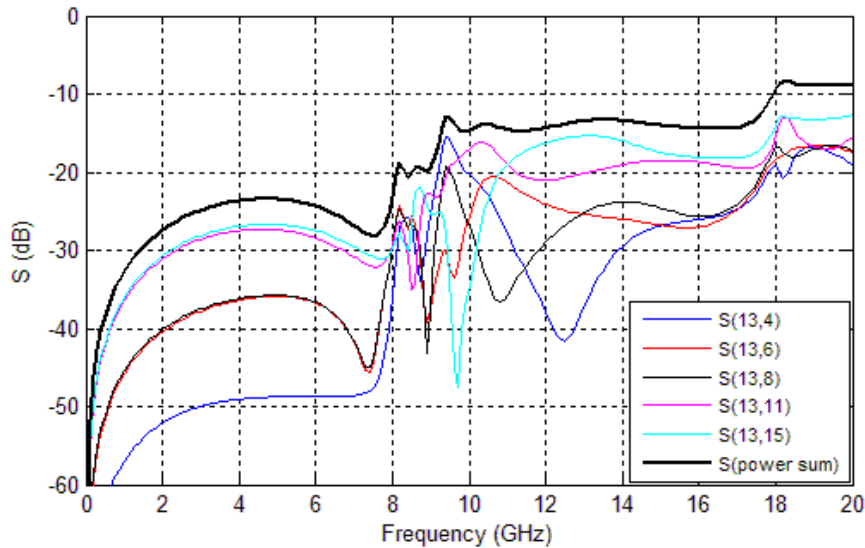


Figure 35 Power Sum of NEXT for port 13 of connector only

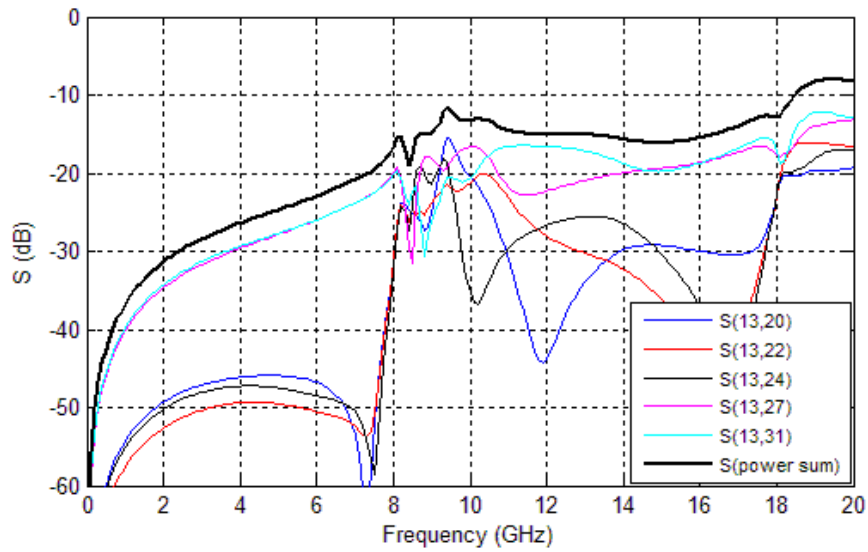


Figure 36 Power Sum of FEXT for port 13 of connector only

4.1.2 W-element Model (PCB trace)

An example of signal traces in the PCB uses the microstrip cross section in Figure 37 for 50 Ohms single-ended impedance. The corresponding W-element model and S parameters are shown in Figure 38 and Figure 39.

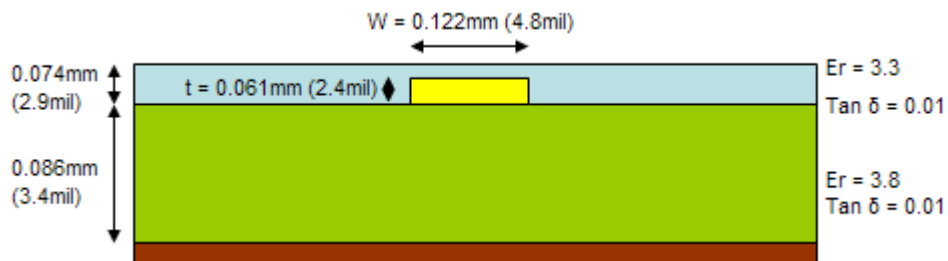


Figure 37 Cross section of single-ended PCB trace

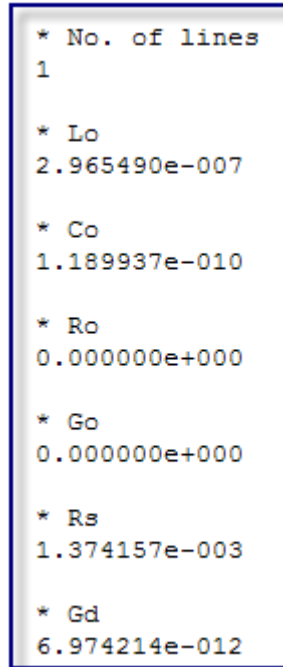


Figure 38 W-element models (in per meter) of Figure 37

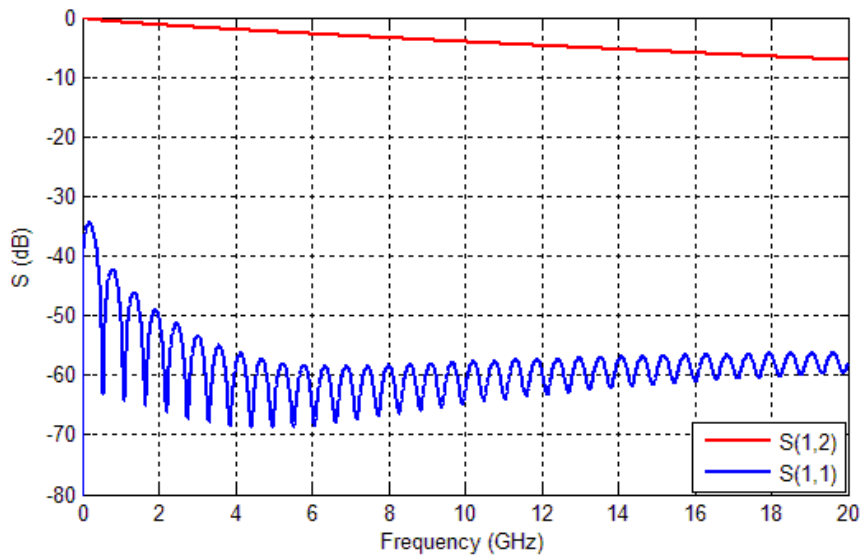


Figure 39 S parameters of 6" PCB trace.

4.2 Time-Domain Simulation

4.2.1 Impedance Profile (connector only)

The impedance profile for port 13 is shown in Figure 40.

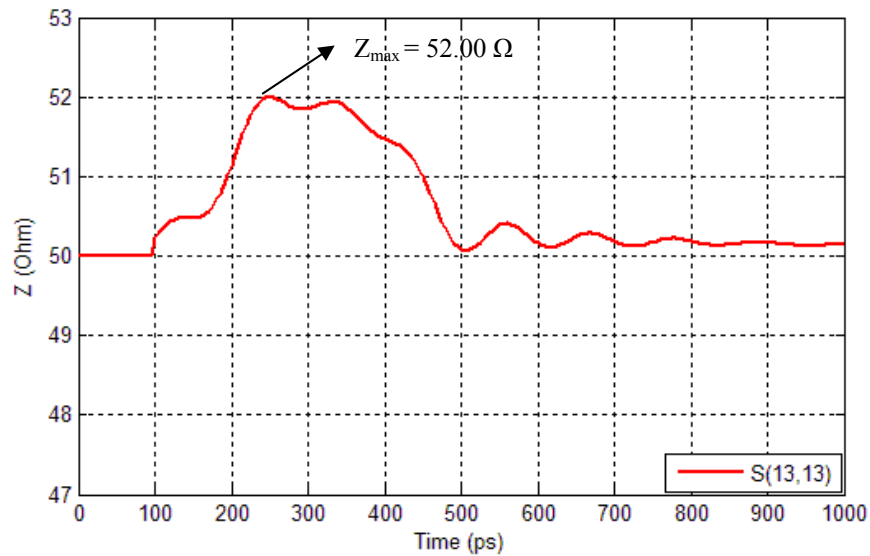


Figure 40 Impedance profile for port 13 of FX10-5mm-noGND @150ps rise time (20% to 80%) and 10GHz_z BW

4.2.2 TDR and TDT waveforms (connector only)

Figure 41 - Figure 43 show the TDR and TDT waveforms at 150ps and 225ps and 300ps rise times (20% to 80%) for port 13 of FX10-5mm-noGND. The worst crosstalk values to the center port are summarized in Table 10.

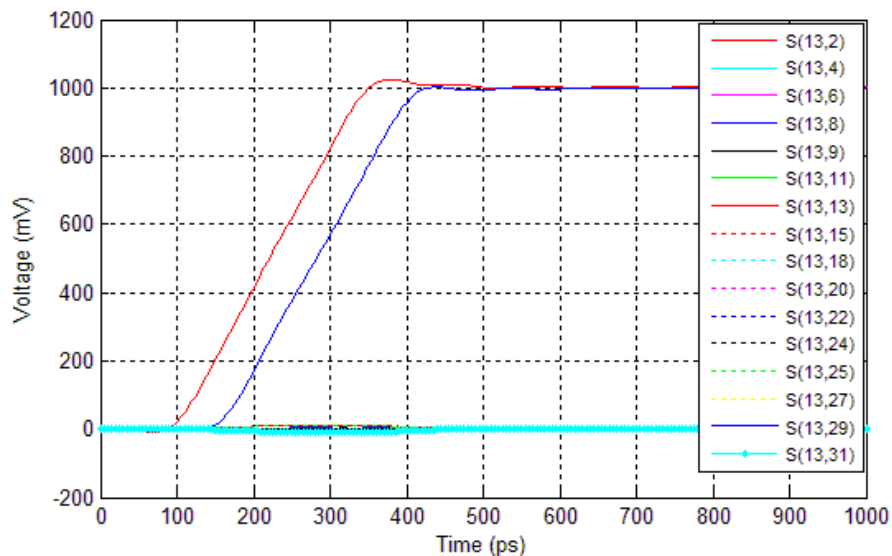


Figure 41 TDR and TDT waveforms @150ps rise time (20% to 80%) and 10GHz_z BW for port 13 of FX10-5mm-noGND

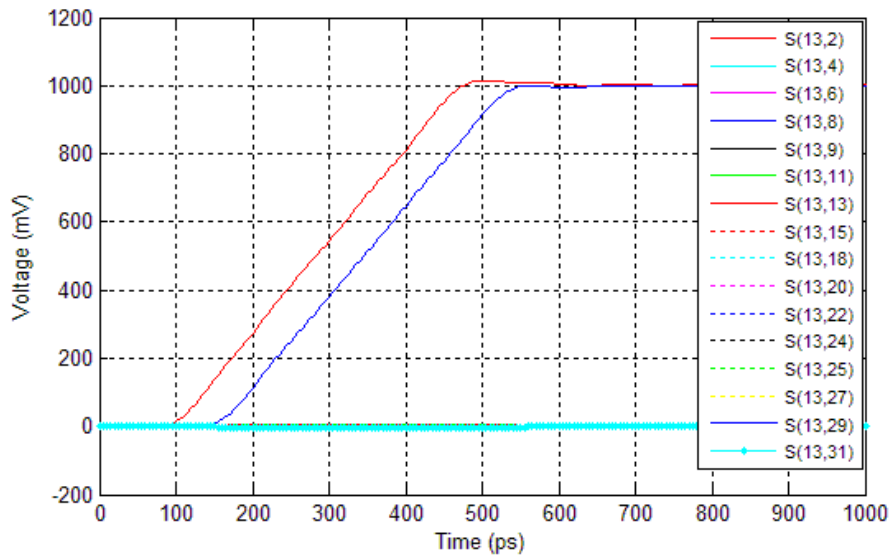


Figure 42 TDR and TDT waveforms @225ps rise time (20% to 80%) and 10GHz BW for port 13 of FX10-5mm-noGND

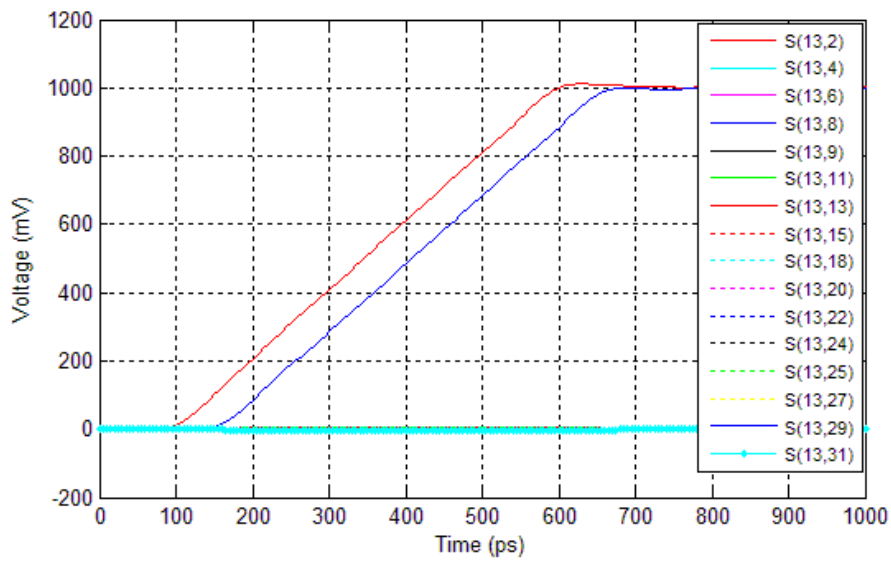


Figure 43 TDR and TDT waveforms @300ps rise time (20% to 80%) and 10GHz BW for port 13 of FX10-5mm-noGND

20% TO 80% RISE TIME (PS)	WORST PAIR-TO-PAIR NEXT (%)	WORST PAIR-TO-PAIR FEXT (%)
150	1.062	0.732
225	0.728	0.507
300	0.556	0.386

Table 10 Summary of Time-domain crosstalk @10GHz BW for port 13 of FX10-5mm-noGND

4.2.3 Time-Domain Crosstalk (connector only)

The total single-ended crosstalk values in % for 150ps (20% to 80%) rise time and 10GHz bandwidth for port 13 is shown in Figure 44.

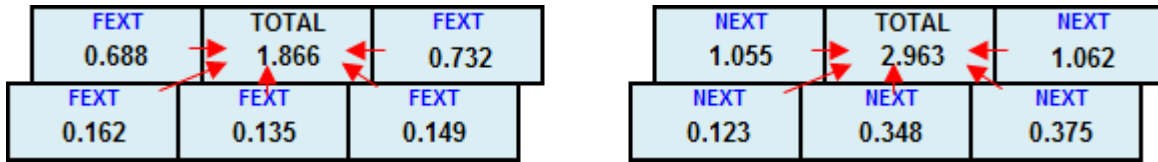


Figure 44 Single-ended crosstalk (in %) from simulations for port 13 using step input with 150ps (20% to 80%) rise time and 10GHz BW

4.2.4 System Voltage and Timing Margins

To demonstrate the FX10’s performance for single-ended signals, we ran simulations with the following setup:

- Ideal voltage source
- FX10 connector
- 152.4mm (6 inches) PCB trace from driver to FX10 connector, and 152.4mm (6 inches) PCB trace from FX10 connector to receiver

Note: Since the time steps used for the simulations were of 5ps, the timing jitter values have an error margin of 5ps. The eye height is defined as the absolute maximum eye opening.

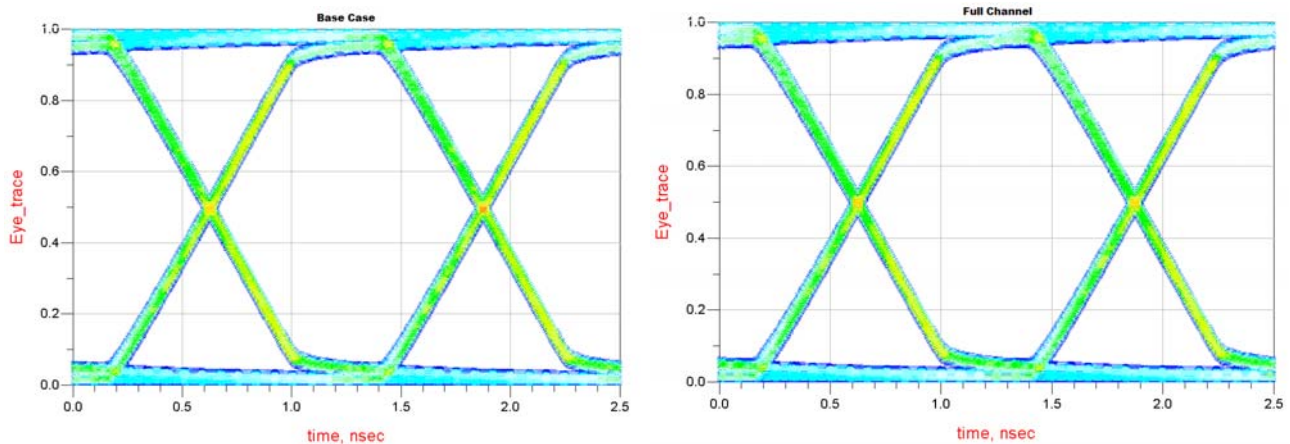


Figure 45 Base case and full channel eye diagram at single-ended receiver input for 800Mbps data rate with 5 FEXT

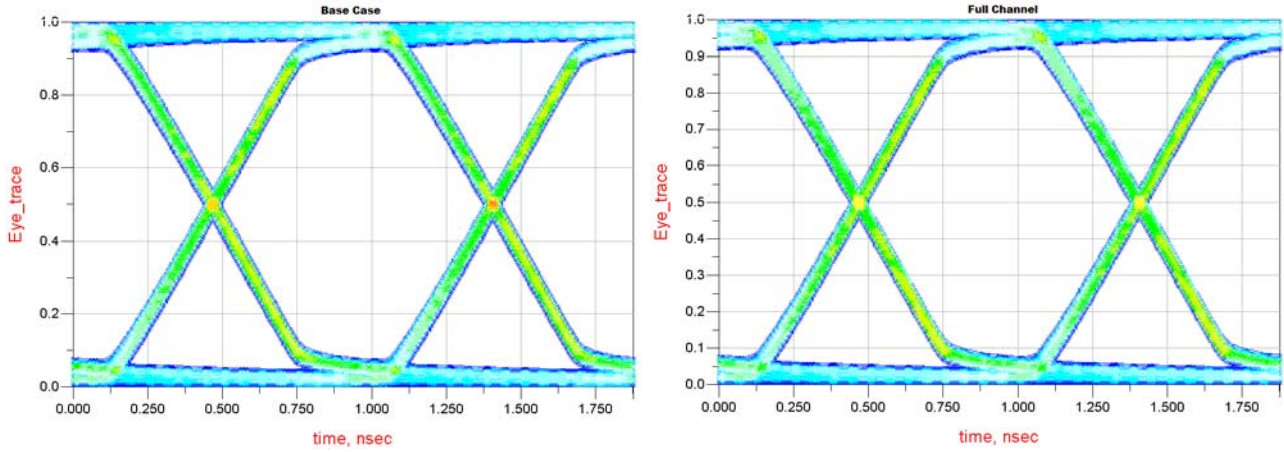


Figure 46 Base case and full channel eye diagram at single-ended receiver input for 1066Mbps data rate with 5 FEXT

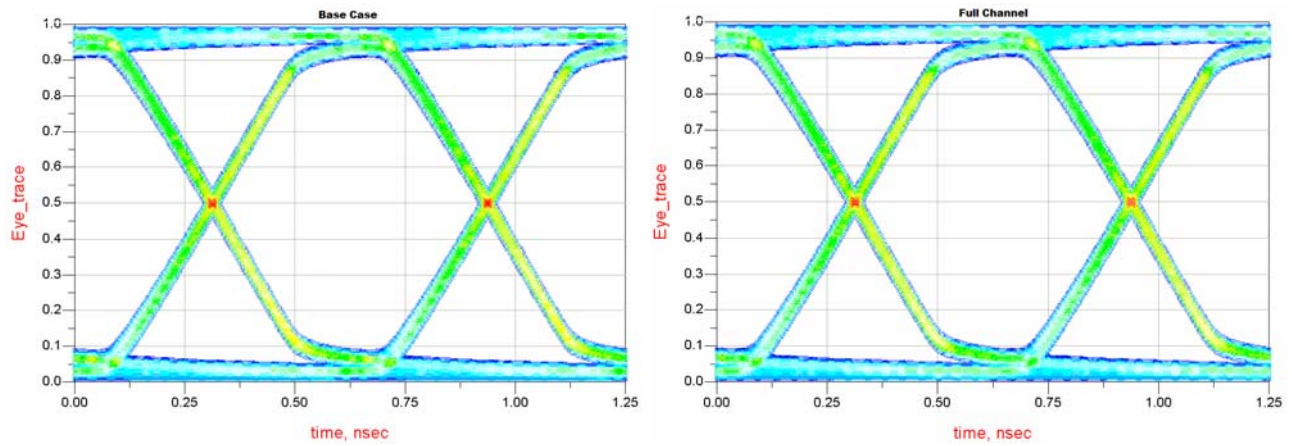


Figure 47 Base case and full channel eye diagram at single-ended receiver input for 1600Mbps data rate with 5 FEXT

Data Rate (Gbps)	Timing Jitter (ps)				Eye Height (mV)			
	FX10	Base Case	Δ FX10	$\frac{\Delta$ FX10 (%)	FX10	Base Case	Δ FX10	$\frac{\Delta$ FX10 (%)
800	38.70	37.61	0.76	0.06	879.13	880.29	-1.16	-0.13
1066	33.70	37.67	-3.97	-0.42	856.46	857.61	-1.15	-0.13
1600	21.87	27.68	-5.81	-0.93	829.43	826.48	2.95	0.36

Table 11 Comparison of eye height and timing fuzz between single-ended full channel and Base Case at the receiver's input with 5 FEXT

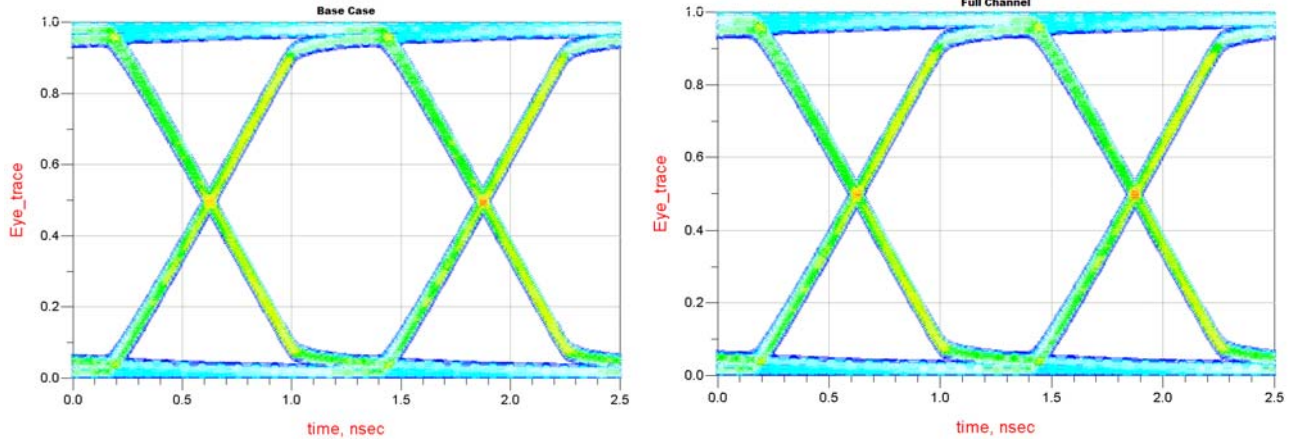


Figure 48 Base case and full channel eye diagram at single-ended receiver input for 800Mbps data rate with 5 NEXT

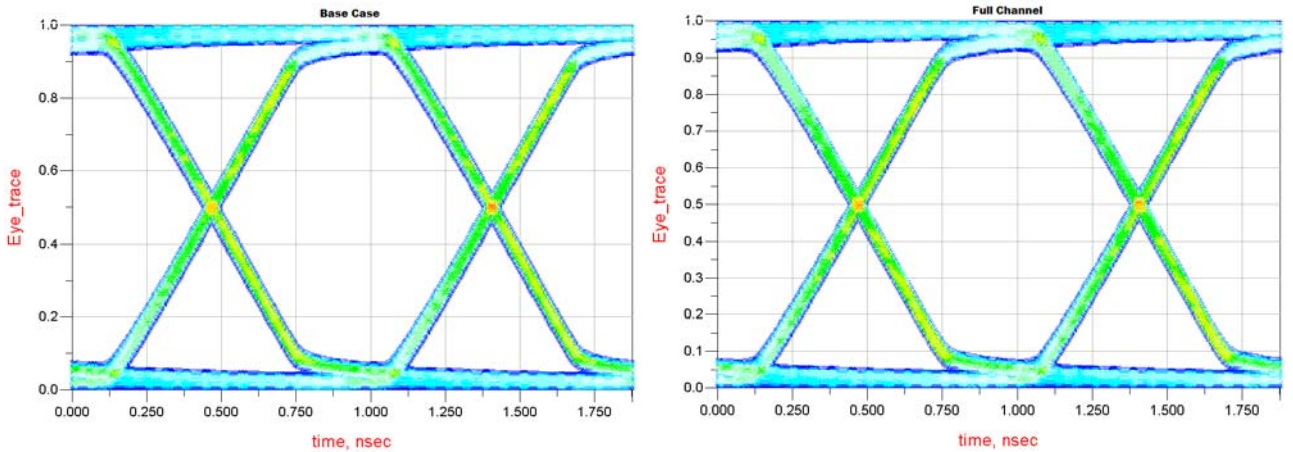


Figure 49 Base case and full channel eye diagram at single-ended receiver input for 1066Mbps data rate with 5 NEXT

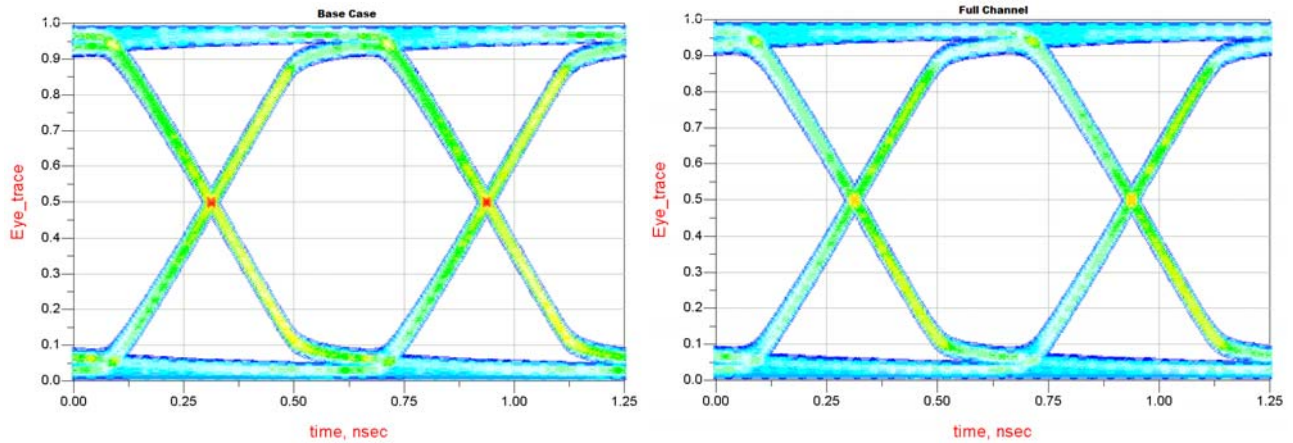


Figure 50 Base case and full channel eye diagram at single-ended receiver input for 1600Mbps data rate with 5 NEXT

Data Rate (Gbps)	Timing Jitter (ps)				Eye Height (mV)			
	FX10	Base Case	Δ FX10	Δ FX10 (%)	FX10	Base Case	Δ FX10	Δ FX10 (%)
800	38.70	37.61	1.09	0.09	877.77	880.29	-2.52	-0.29
1066	33.54	37.67	-4.13	-0.44	854.48	857.61	-3.13	-0.36
1600	21.99	27.68	-5.69	-0.91	827.24	826.48	0.76	0.09

Table 12 Comparison of eye height and timing jitter between single-ended full channel and Base Case at the receiver's input with 5 NEXT

5. Measurement

5.1 Measurement Setup

To measure the connector's performance directly we pre-characterized and de-embedded the test boards to eliminate the effects of SMAs, traces and vias. The characterization boards were designed to have minimal effect on the connector's performance. The traces have controlled impedance of 50Ω and coplanar traces were used to minimize the crosstalk from trace to trace. The measurement setup is shown in Figure 51.

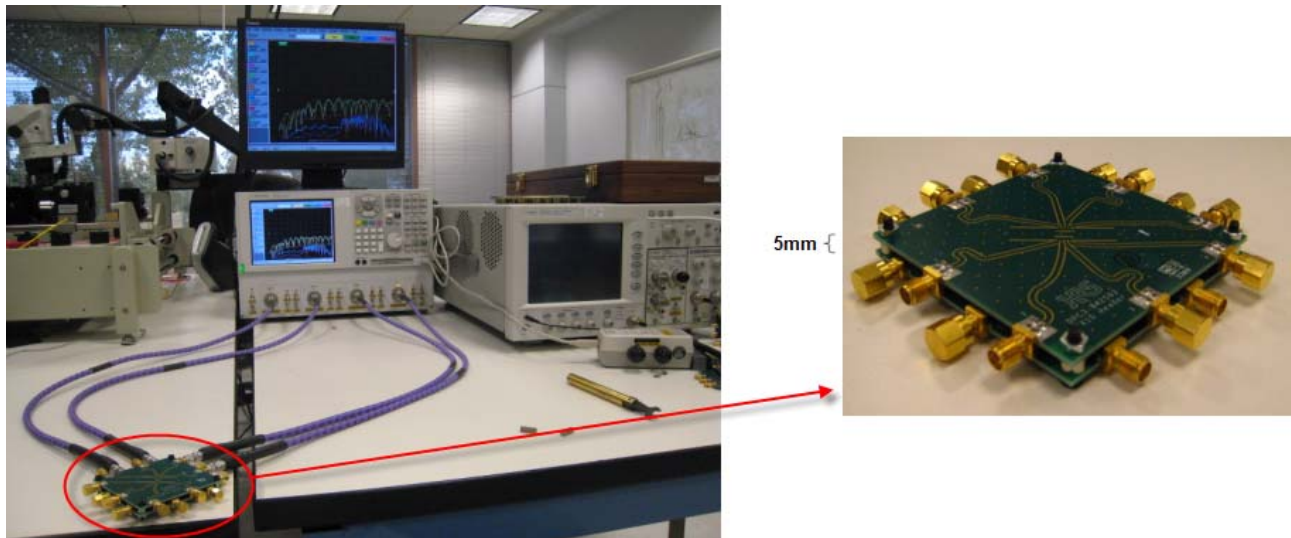


Figure 51 Measurement setup

The FX10-5mm-noGND connector was also tested in a demo board with 8'' channel of 63mil FR406 board, mid-layer routing, and 4-aggressor crosstalk, as shown in Figure 52.

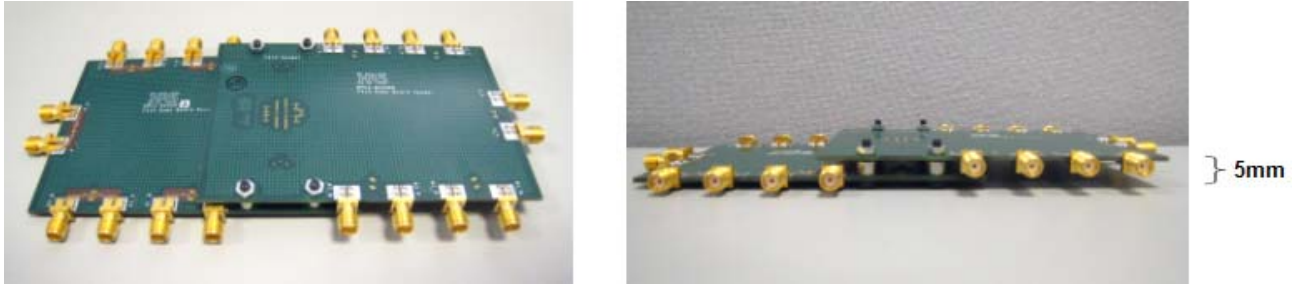


Figure 52 Demo board setup

5.2 Differential Signals

5.2.1 Measurement vs. Simulation Correlation (connector only)

Figure 54 and Figure 55 show the measurement vs. simulation correlation of insertion loss (IL), return loss (RL) and differential S parameters (SDD) between four nearest neighboring pairs for pair 3 (as shown in Figure 53). Good correlation was observed for all IL, RL, near-end crosstalk (NEXT), and far-end crosstalk (FEXT).

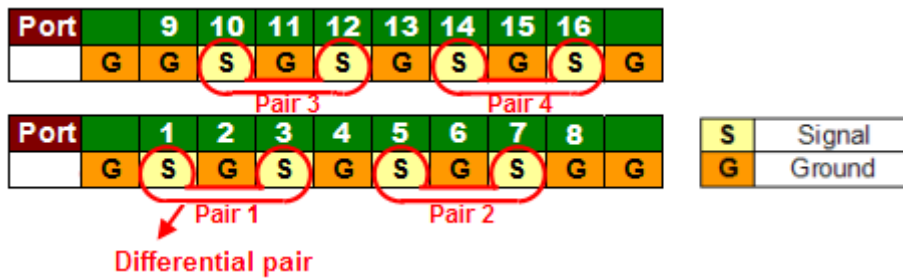
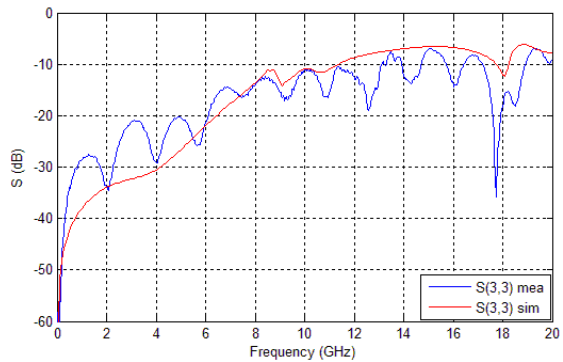
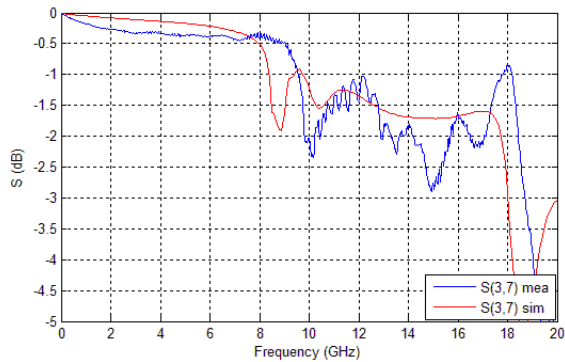


Figure 53 FX10-5mm-noGND pin assignment



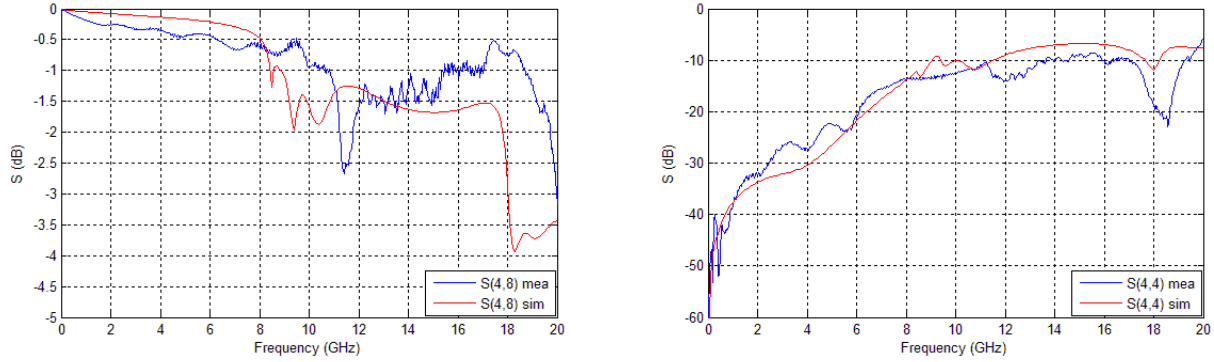
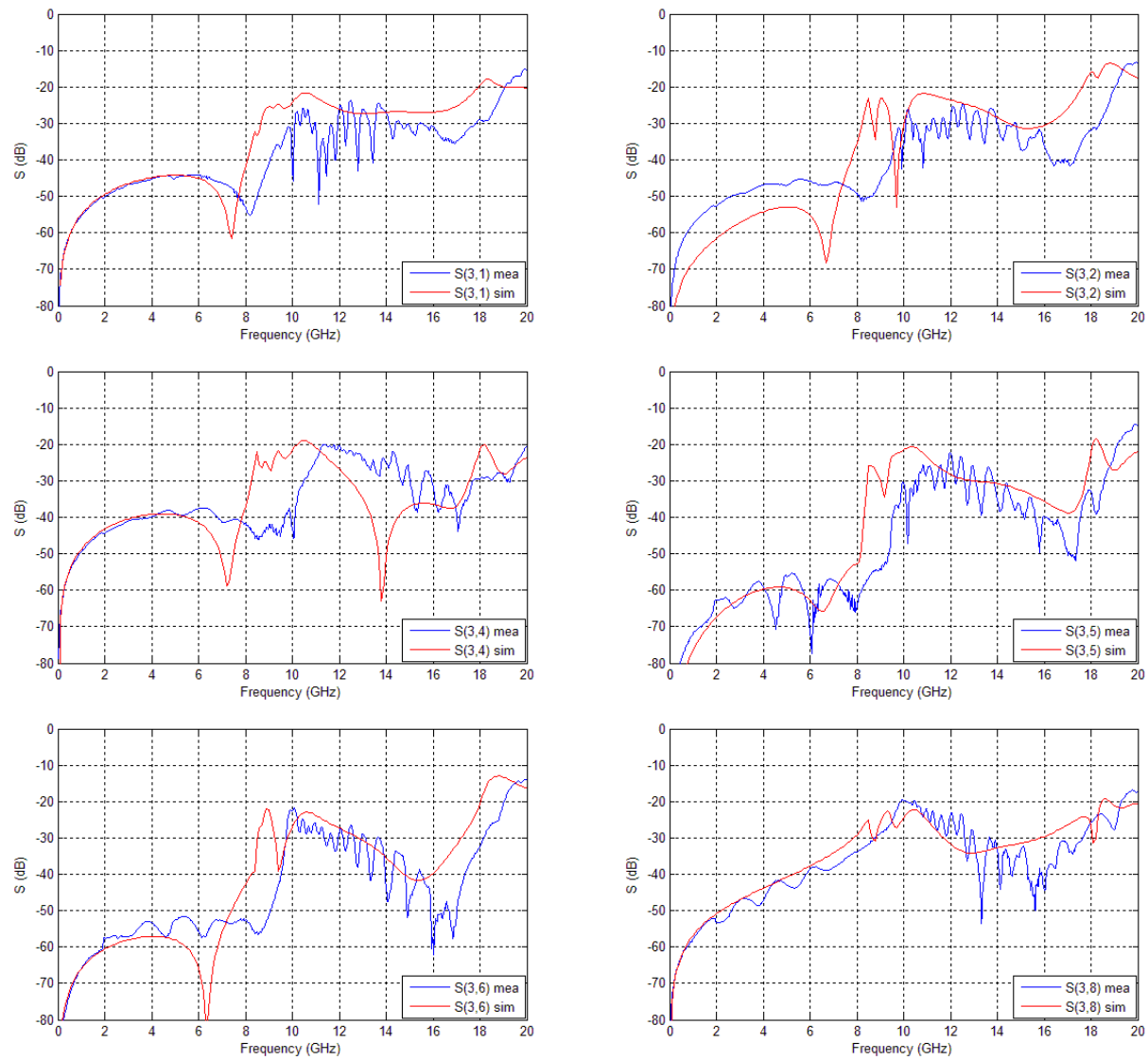


Figure 54 Measurement vs. simulation correlation of IL and RL for pair 3 and pair 4 (for FX10-5mm-noGND) as shown in Figure 53



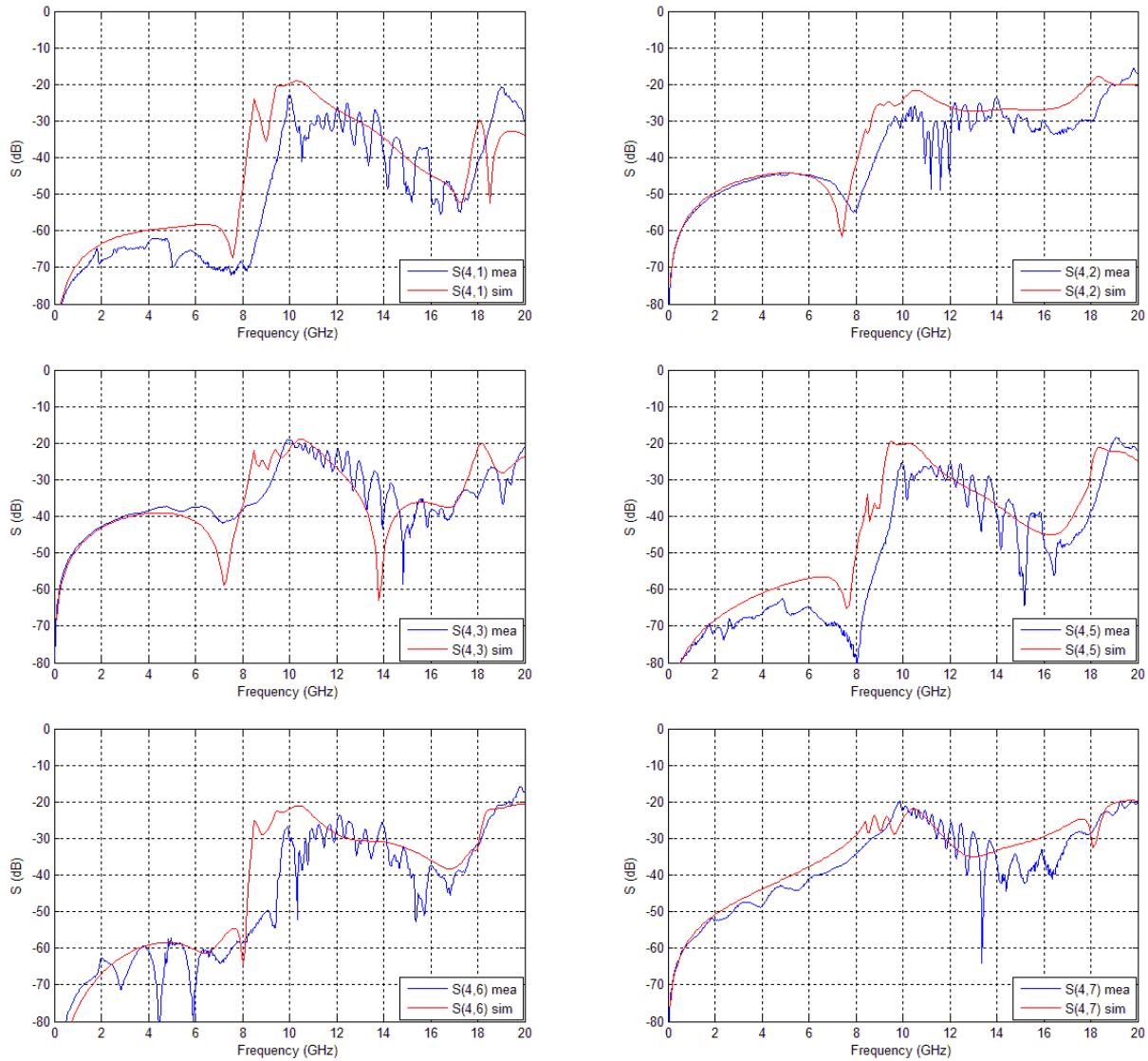


Figure 55 Measurement vs. simulation correlation of differential S parameters between two nearest neighbors for pair 3 and 4 (for FX10-5mm-noGND) as shown in Figure 53

5.2.2 Time-Domain NEXT and FEXT

Differential NEXT and FEXT were measured for 4 surrounding neighbors of the center differential pair and converted into time-domain data. Figure 56 shows the maximum differential NEXT and FEXT (in %) from each neighbor using step input at 60ps (20% to 80%) rise time and 20 GHz bandwidth. The center box corresponds to the absolute sum of NEXT and FEXT from the 4 surrounding pairs.

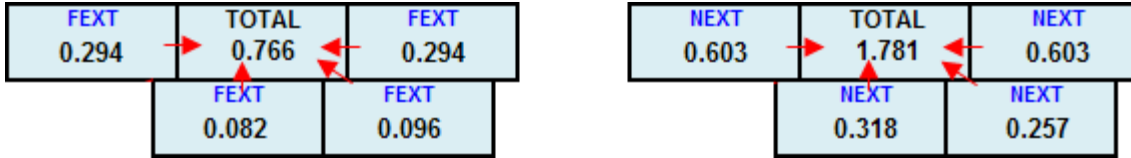


Figure 56 Differential crosstalk (in %) from measurements using step input with 60ps (20% to 80%) rise time and 20GHz BW for the center pair and 4 aggressors

5.2.3 Impedance profile

From the time domain results, the impedance profile is extracted and compared with simulation results, as shown in Figure 57.

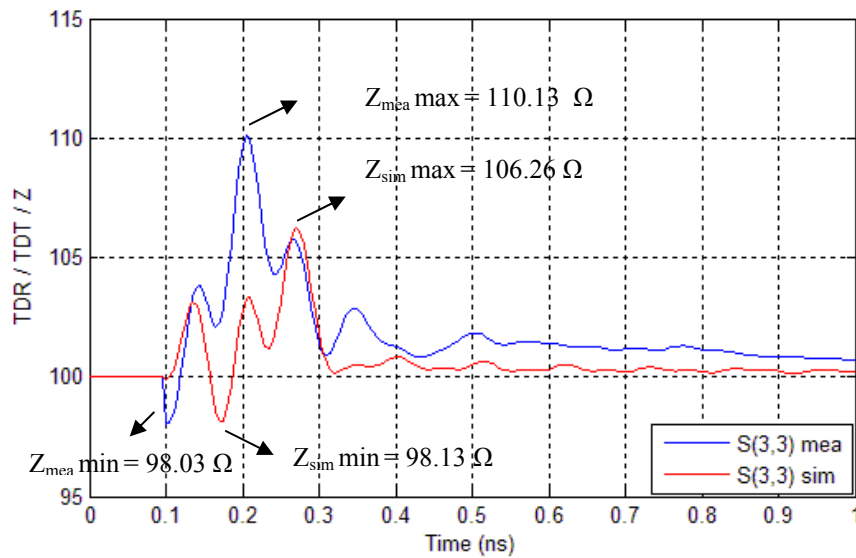


Figure 57 Impedance profile comparison between measurements and simulation for center differential pair 3 @60ps rise time (20% to 80%) and 20GHz BW

5.3 Single-ended Signals

5.3.1 Measurement vs. Simulation Correlation (connector only)

Figure 59 and Figure 60 show the measurement vs. simulation correlation of insertion loss (IL), return loss (RL) and single-ended S parameters (SDD) between four nearest neighboring pairs for port 13 (as shown in Figure 58). Good correlation was observed for all IL, RL, near-end crosstalk (NEXT), and far-end crosstalk (FEXT).

Port		9	10	11	12	13	14	15	16	
	G	S	G	S	G	S	G	S	G	G

Port		1	2	3	4	5	6	7	8	
	G	G	S	G	S	G	S	G	S	G

S	Signal
G	Ground

Figure 58 FX10-5mm-noGND single-ended pin assignment

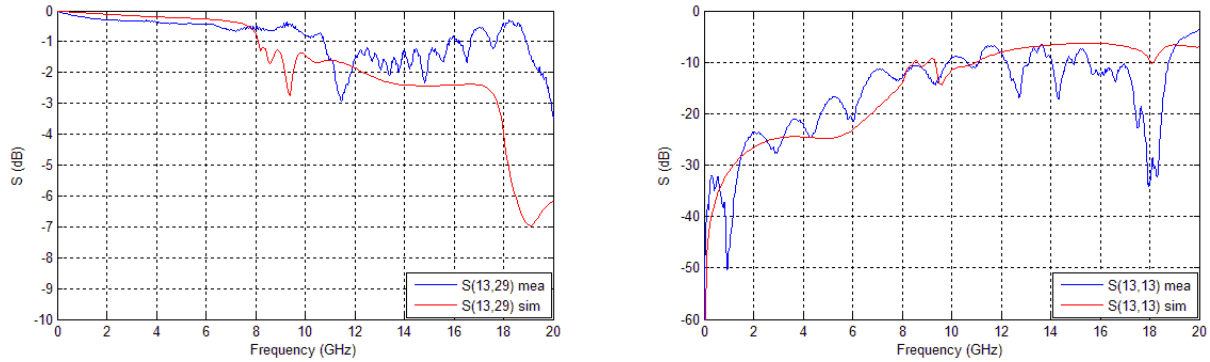
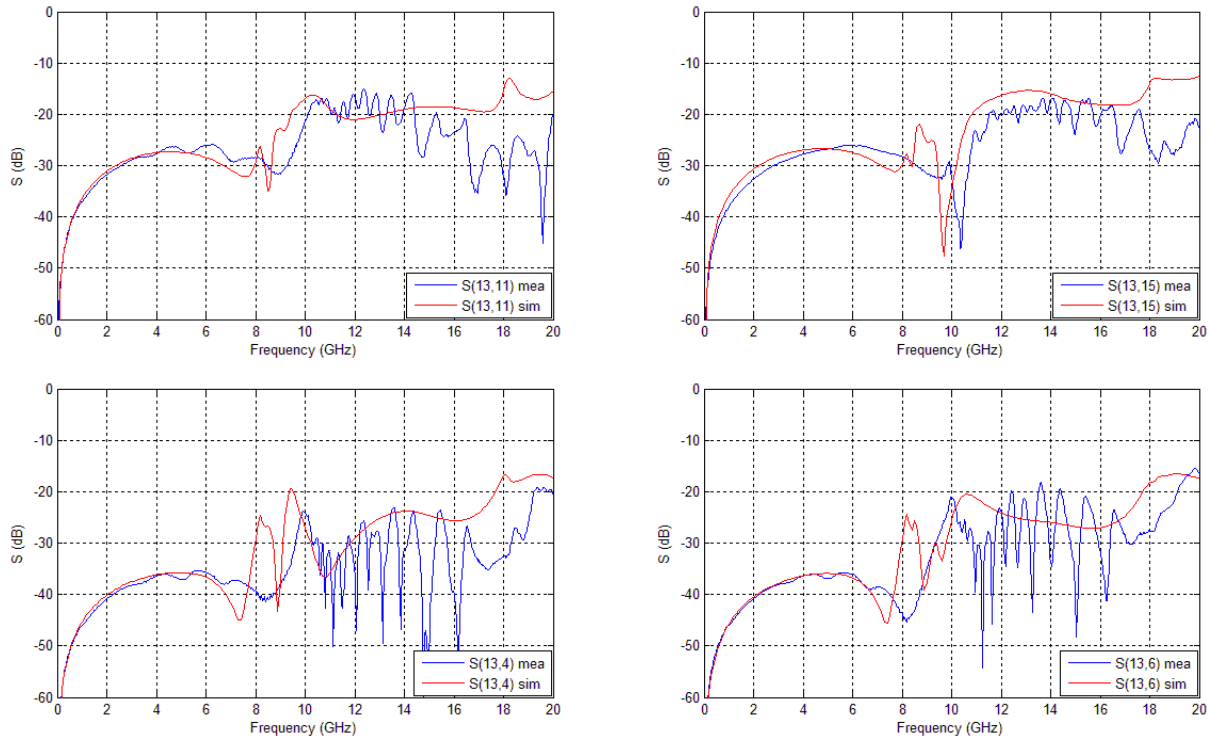


Figure 59 Measurement vs. simulation correlation of IL and RL for port 13 (for FX10-5mm-noGND) as shown in Figure 58



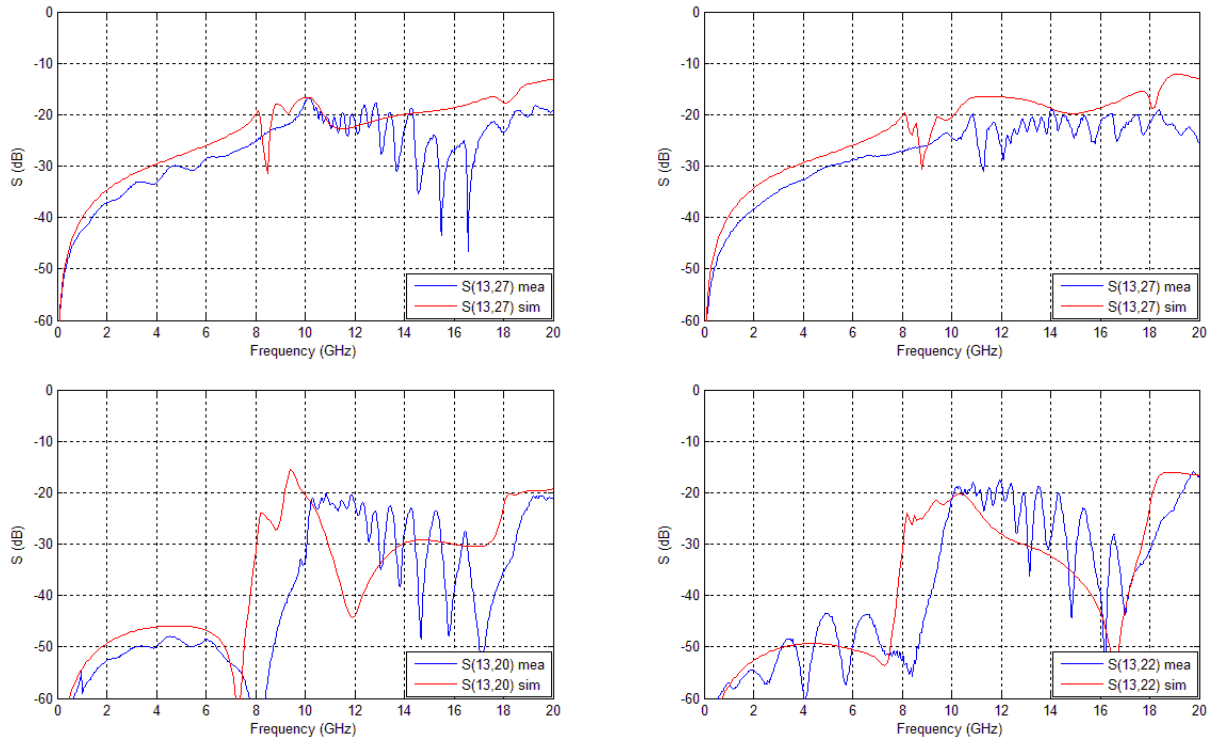


Figure 60 Measurement vs. simulation correlation of single-ended S parameters between four nearest neighbors for port 13 (for FX10-5mm-noGND) as shown in Figure 58

5.3.2 Time-Domain NEXT and FEXT

Single-ended NEXT and FEXT were measured for 4 surrounding neighbors of the center single-ended port 13 and converted into time-domain data. Figure 61 shows the maximum differential NEXT and FEXT (in %) from each neighbor using step input at 150ps (20% to 80%) rise time with 10 GHz bandwidth. The center box corresponds to the absolute sum of NEXT and FEXT from the 4 surrounding single-ended signal ports.

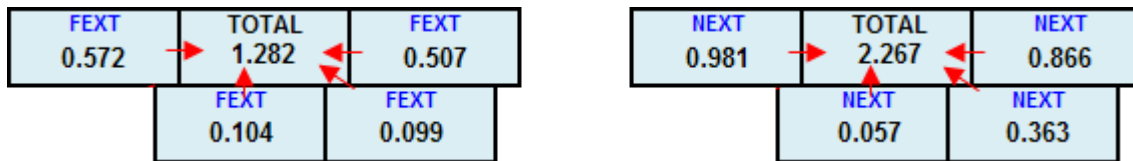


Figure 61 Single-ended crosstalk (in %) from measurements using step input with 150ps (20% to 80%) rise time and 10GHz BW for the center port and 4 aggressors

5.3.3 Impedance profile

From the time domain results, the impedance profile is extracted and compared with simulation results, as shown in Figure 62.

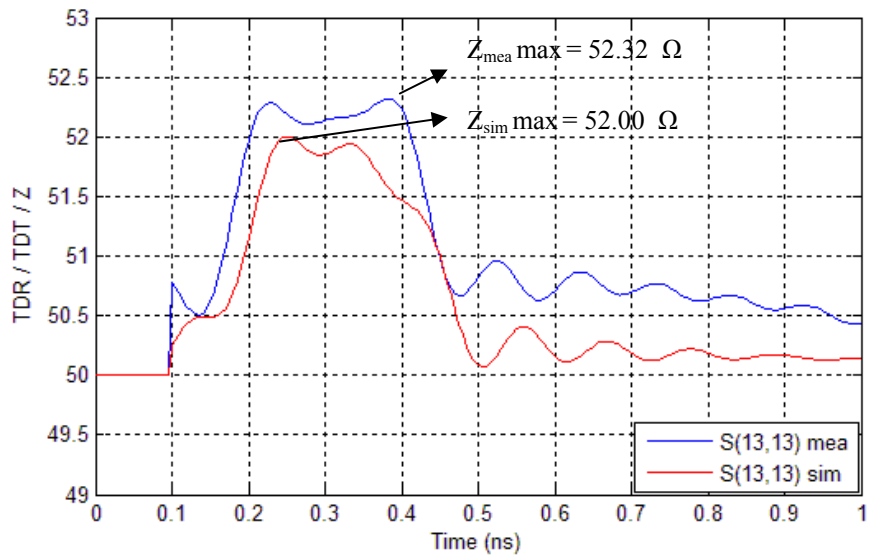


Figure 62 Impedance profile comparison between measurements and simulation port 13 @150ps rise time (20% to 80%) and 10GHz BW

6. Appendix

Figure 63 shows the ADS schematic setup for eye diagram simulations. For each data rate, 1,000 bits were simulated. Crosstalk values for each pair to the center pair were extracted and added to the final voltage seen at the receiver of the center pair. The rise and fall times used are given by:

$$RiseTime_{0\% \sim 100\%} = \frac{BitTime \times 40\%}{60\%}$$

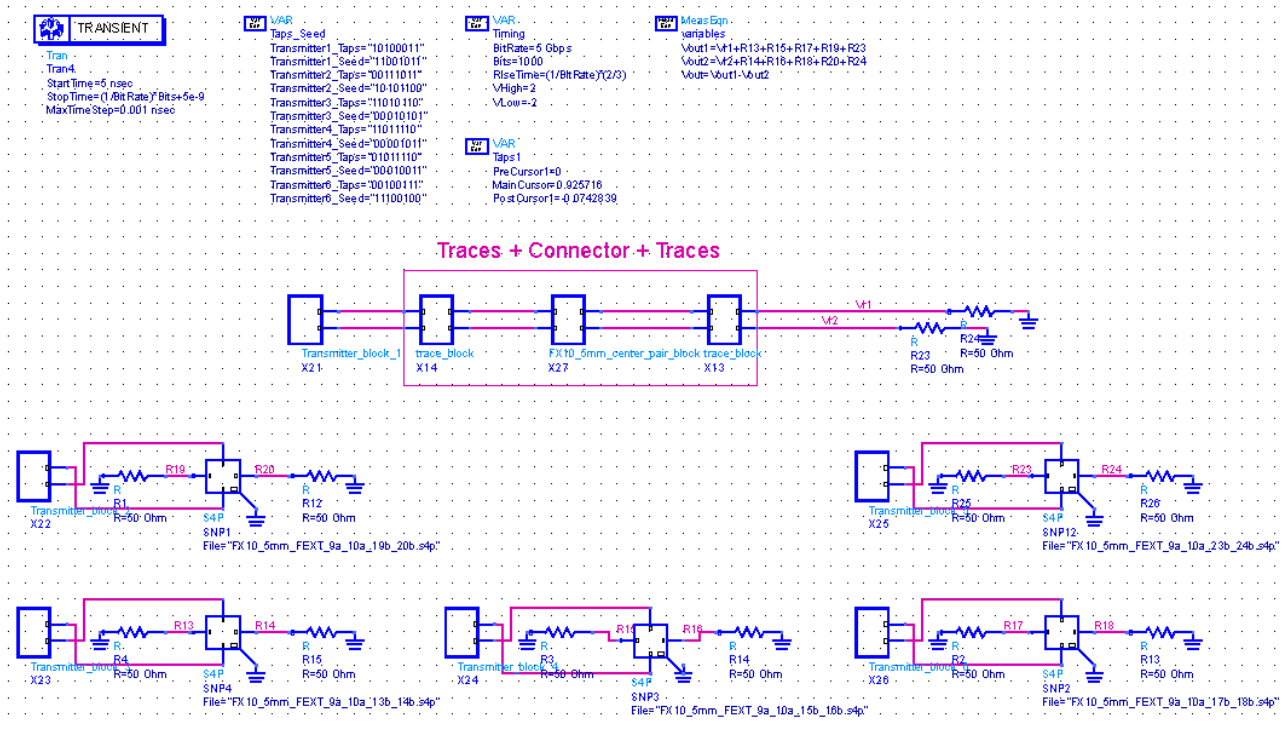


Figure 63 Full channel with 5 FEXT setup

Figure 64 and Figure 65 show the ADS schematic for the transmitter circuit with 3-tap and 7-tap transmitter equalization setup. Each transmitter has a different bit pattern with a maximum register length of 32. The differential peak-to-peak voltage at the output of the transmitter block is -1V to 1V.

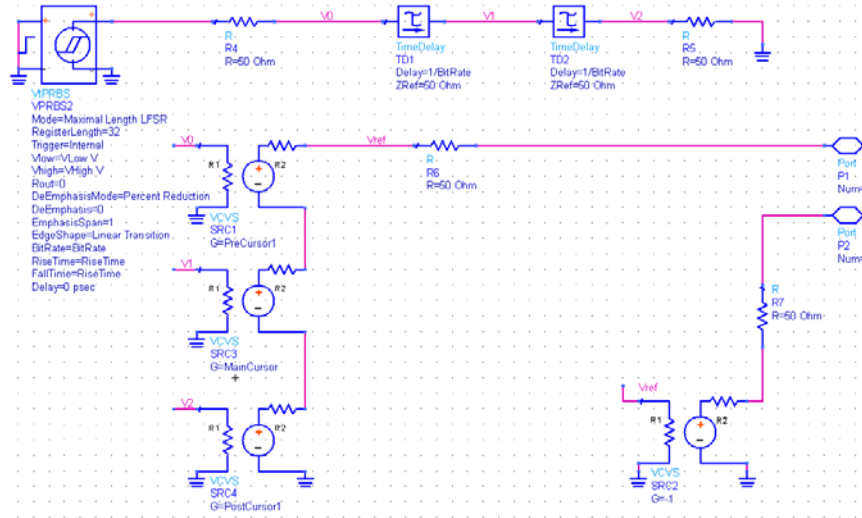


Figure 64 3-tap transmitter equalization setup

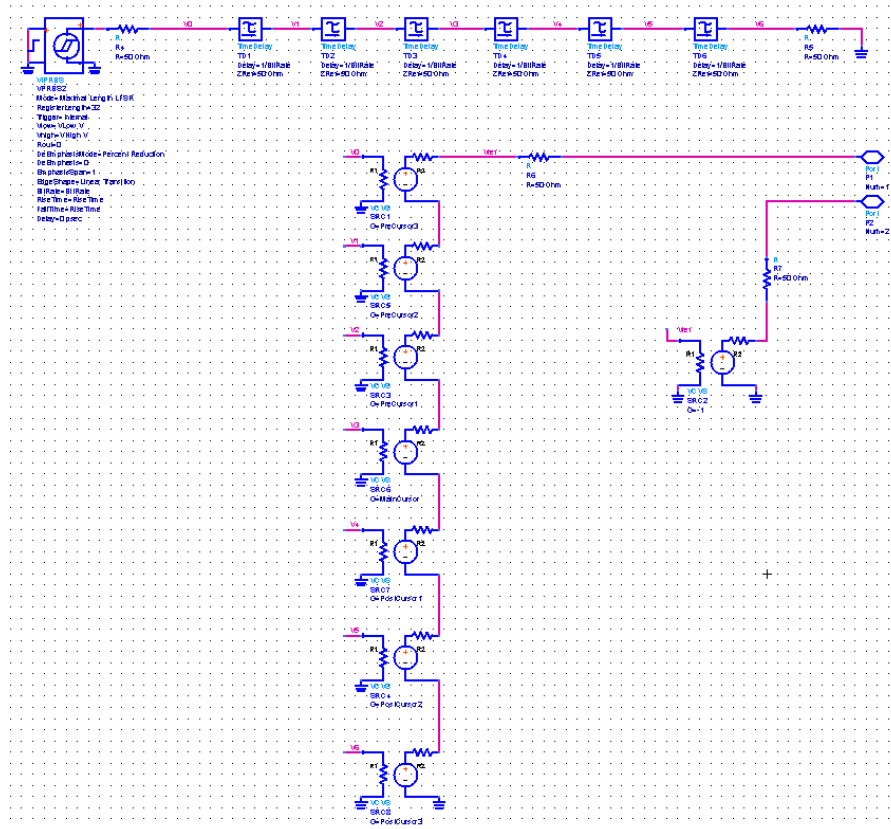


Figure 65 7-tap transmitter equalization setup