

# Recommendations for USB 3.0 Test Fixture

July 23rd, 2010



**HIROSE ELECTRIC**

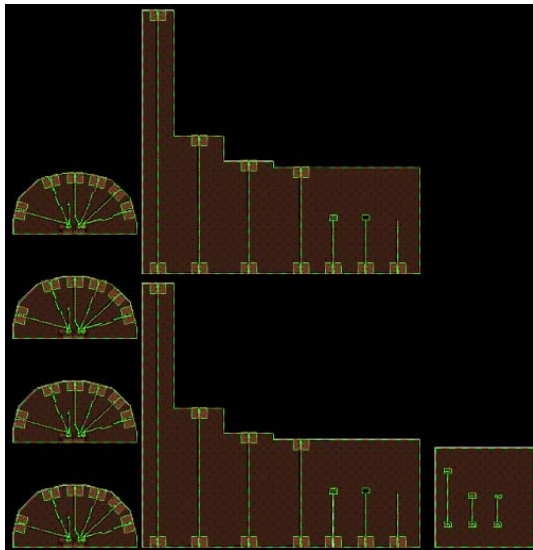
# Agenda

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- Objective
- Recommendations for PCB design
  - Connector footprint area
  - General test board considerations
- Summary

# Objective

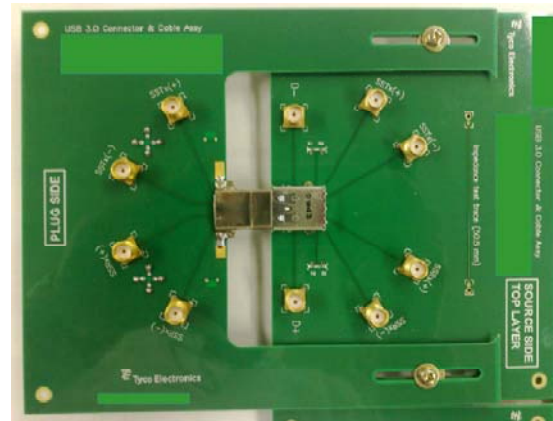
- Contribute some recommendations to improve USB connector characterization test fixtures.
- Design a suitable characterization PCB which has minimal effects on measurement results of micro-B USB connector.



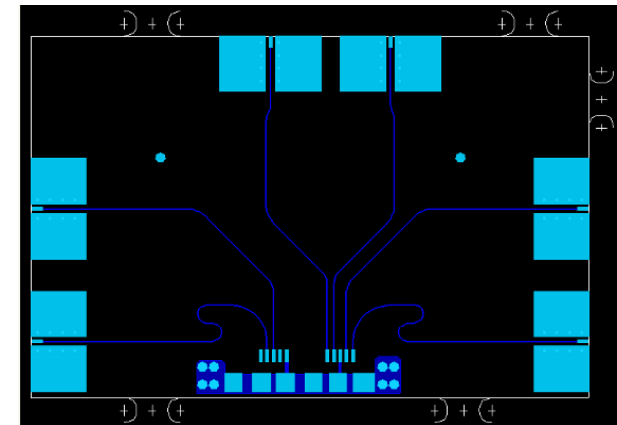
*Hirose PCB layout*



*Hirose test board*



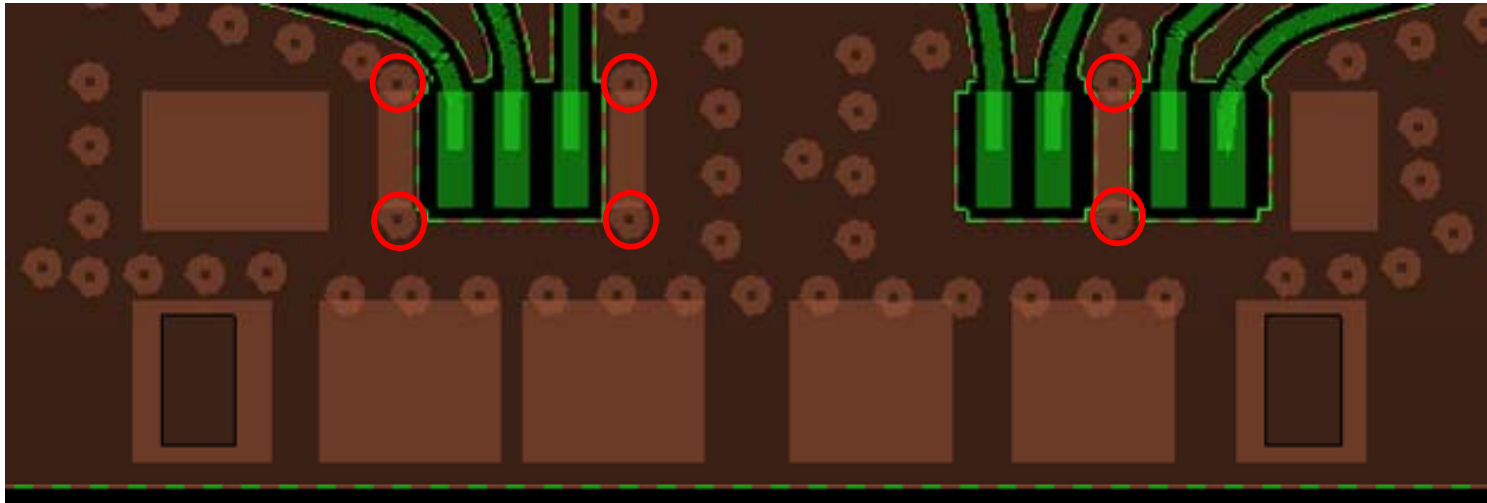
*Tyco test board*



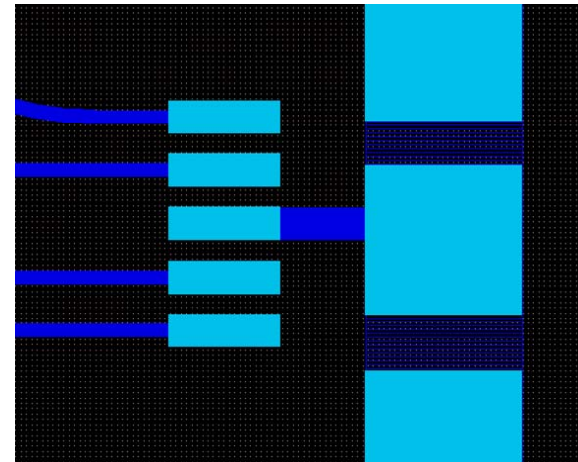
*Intel PCB layout*

# Ground vias near ground pins

- Adding ground vias near the ground pins will ensure good ground reference at the connector.

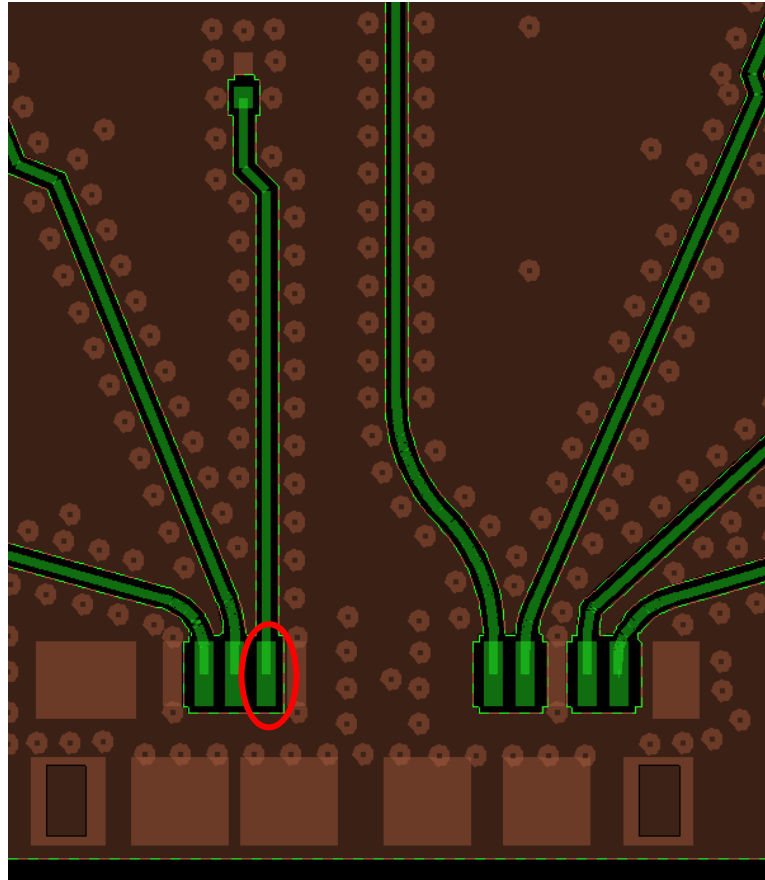


*Grounding pins using a trace creates a longer return path.*



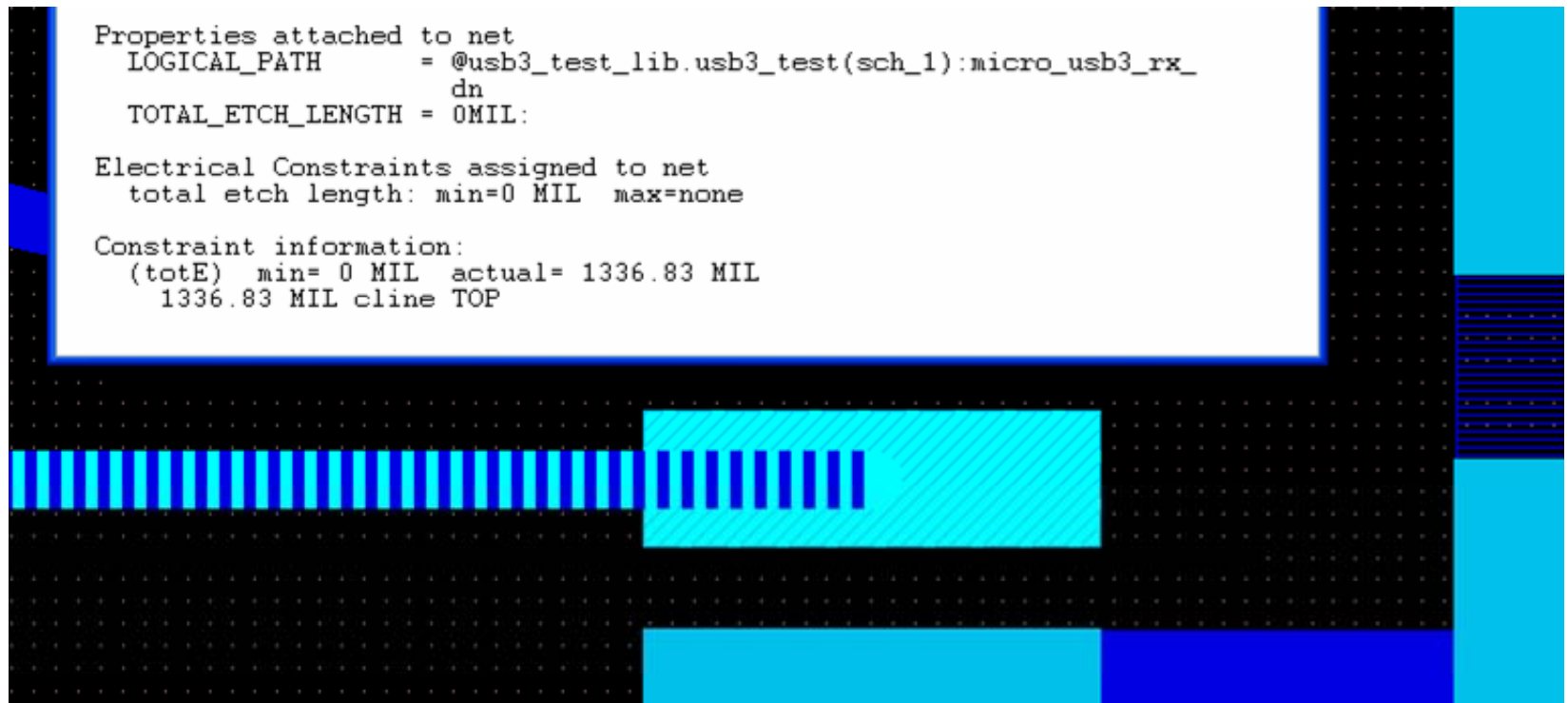
## Terminate unused pins

- Terminating unused pins mimics actual application and minimizes possibility of resonance caused by unused pins.



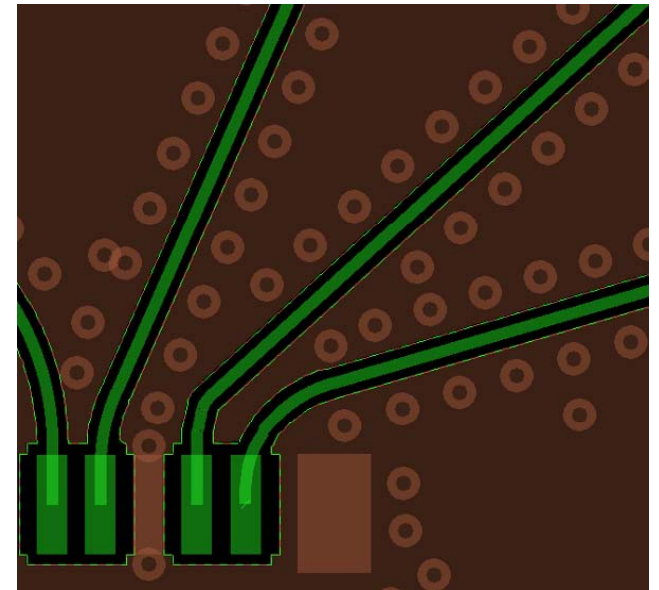
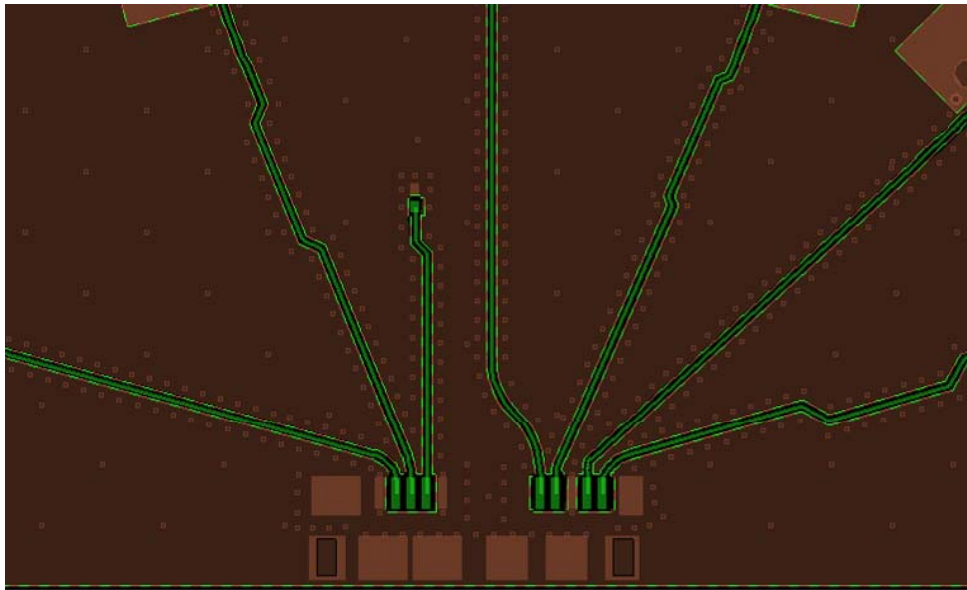
# Reference trace length

- PCB layout needs to consider the reference trace length from SMA to the edge of the connector pad.
  - Routing traces to the middle of a connector pad can cause a 30 mil deviation from the actual reference length.

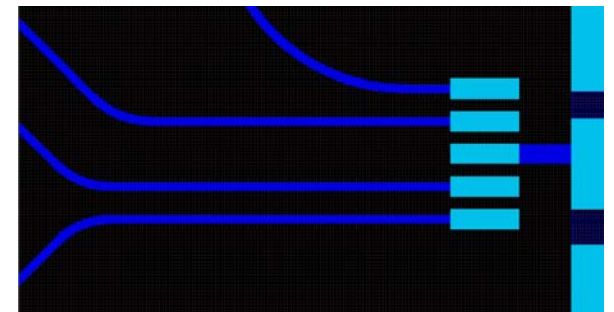


# Minimize trace crosstalk

- Space out PCB traces
- Use coplanar traces to minimize crosstalk
- Use stitching vias to prevent resonance

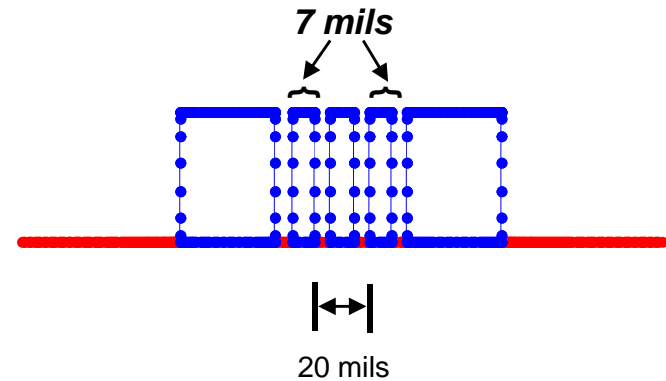
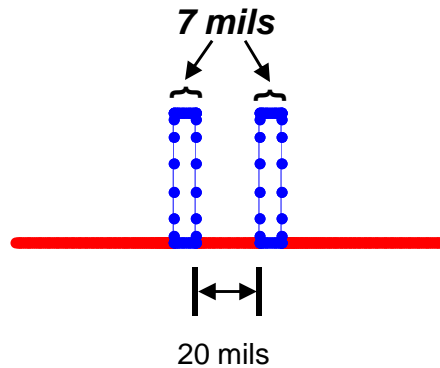


*Having traces running parallel to each other can cause undesirable crosstalk.*



# Minimizing trace crosstalk

- Coplanar traces help to reduce measurement crosstalk.



```

35
36 Voltage Coupling Matrix - Saturated voltage
37 1.000000e+000 1.417177e-002
38 1.417177e-002 1.000000e+000
39
    
```

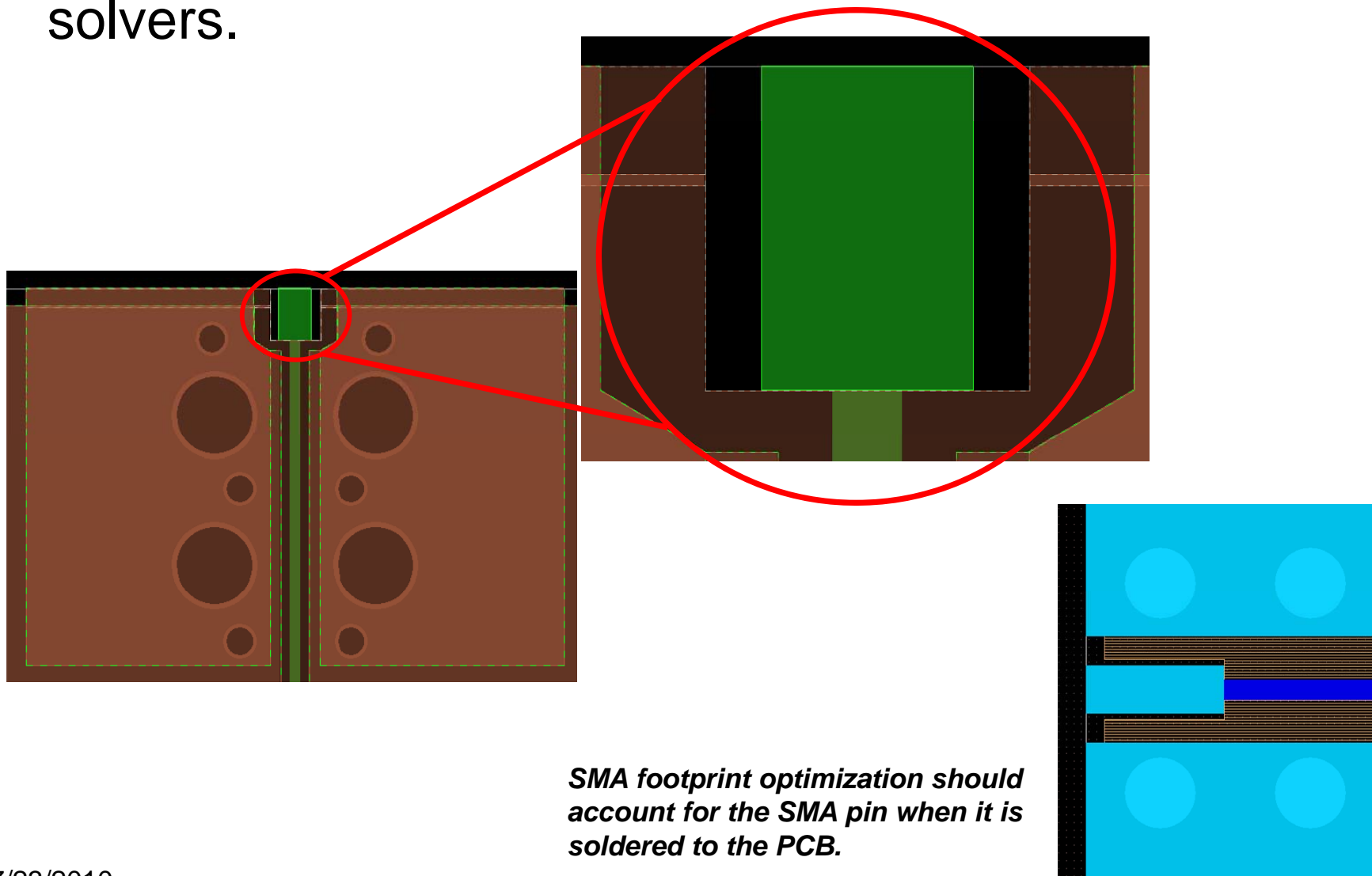
```

35
36 Voltage Coupling Matrix - Saturated voltage
37 1.000000e+000 6.019990e-003
38 6.019990e-003 1.000000e+000
39
    
```

**1.42% coupling vs. 0.6% coupling  
between traces**

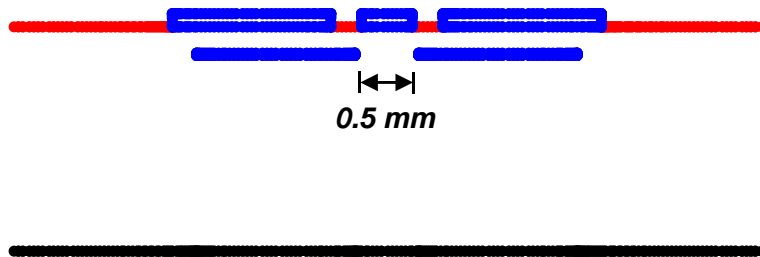
# SMA footprint

- SMA footprints can be optimized to minimize impedance discontinuities at the launch using 2D field solvers.



# SMA footprint optimization

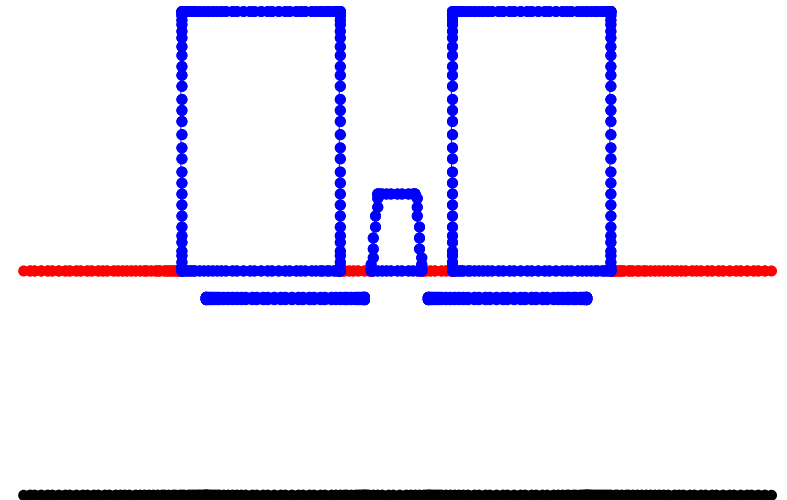
- Footprints should be optimized with the components taken in to consideration.



```

7
8 Lossy Characteristic Impedance Matrix [ZC] (Ohm)
9 4.955260e+001+i*-1.661388e-002
10
    
```

*Current footprint gives 50 ohms without SMA pin*



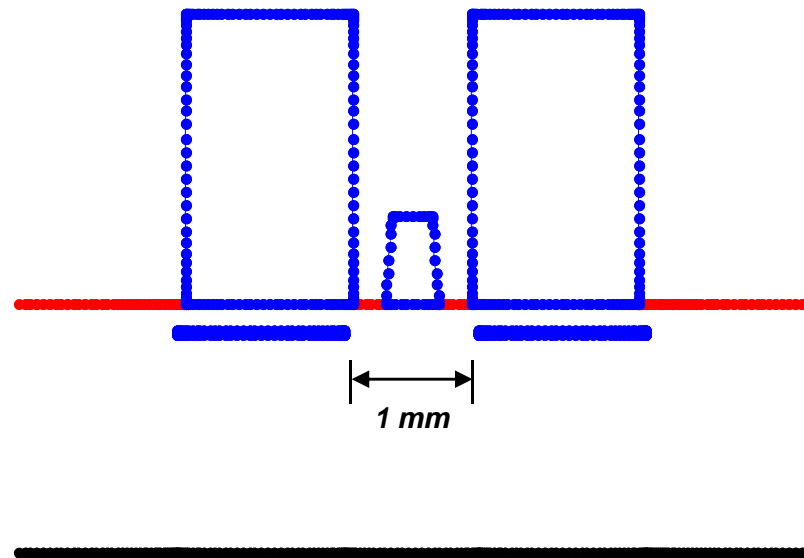
```

7
8 Lossy Characteristic Impedance Matrix [ZC] (Ohm)
9 3.828148e+001+i*-6.504972e-003
10
    
```

*SMA footprint with SMA pin would actually be around 40 ohms*

# SMA footprint optimization

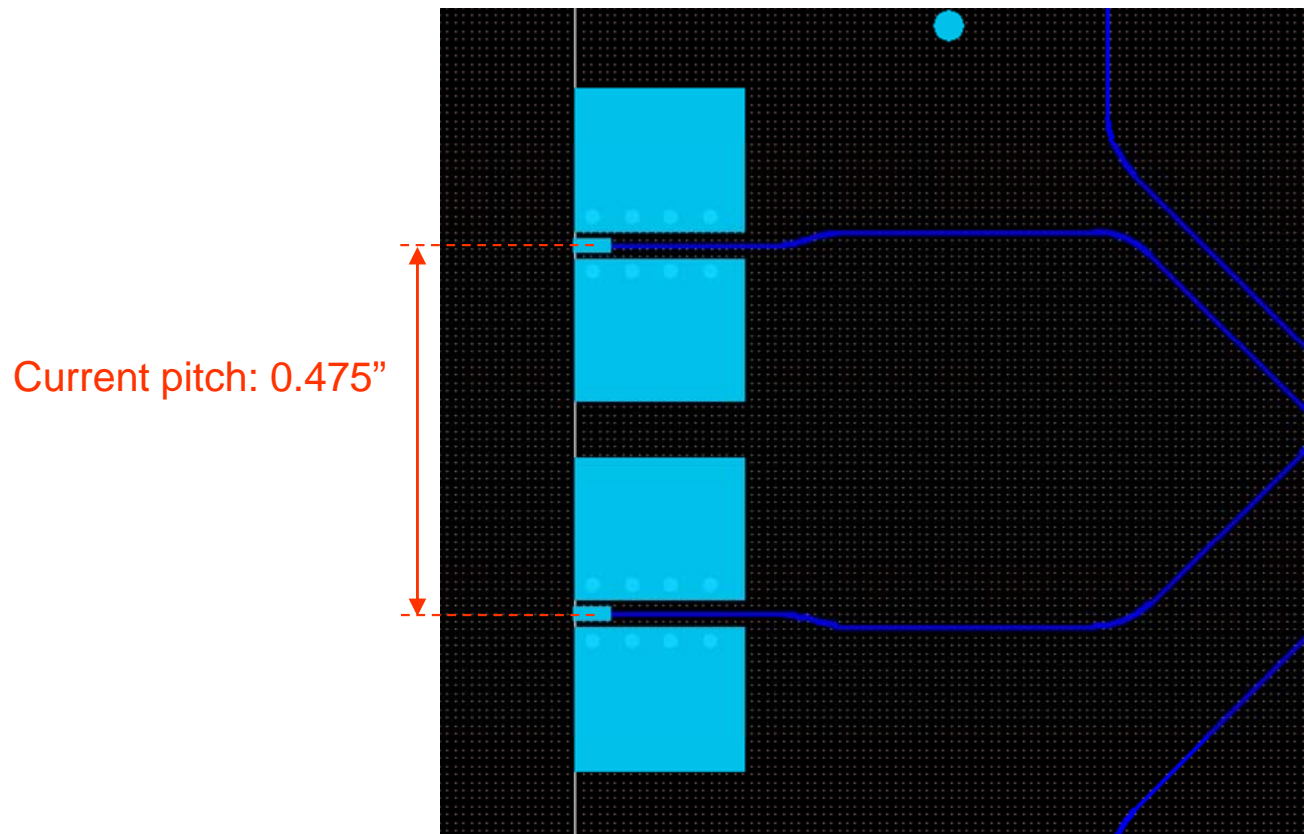
- Designing a cutout in the ground plane at the SMA pin makes it possible to match the impedance of the PCB trace.



```
7  
8 Lossy Characteristic Impedance Matrix [ZC] (Ohm)  
9 4.904986e+001+i* 3.066134e-002  
10
```

## SMA spacing

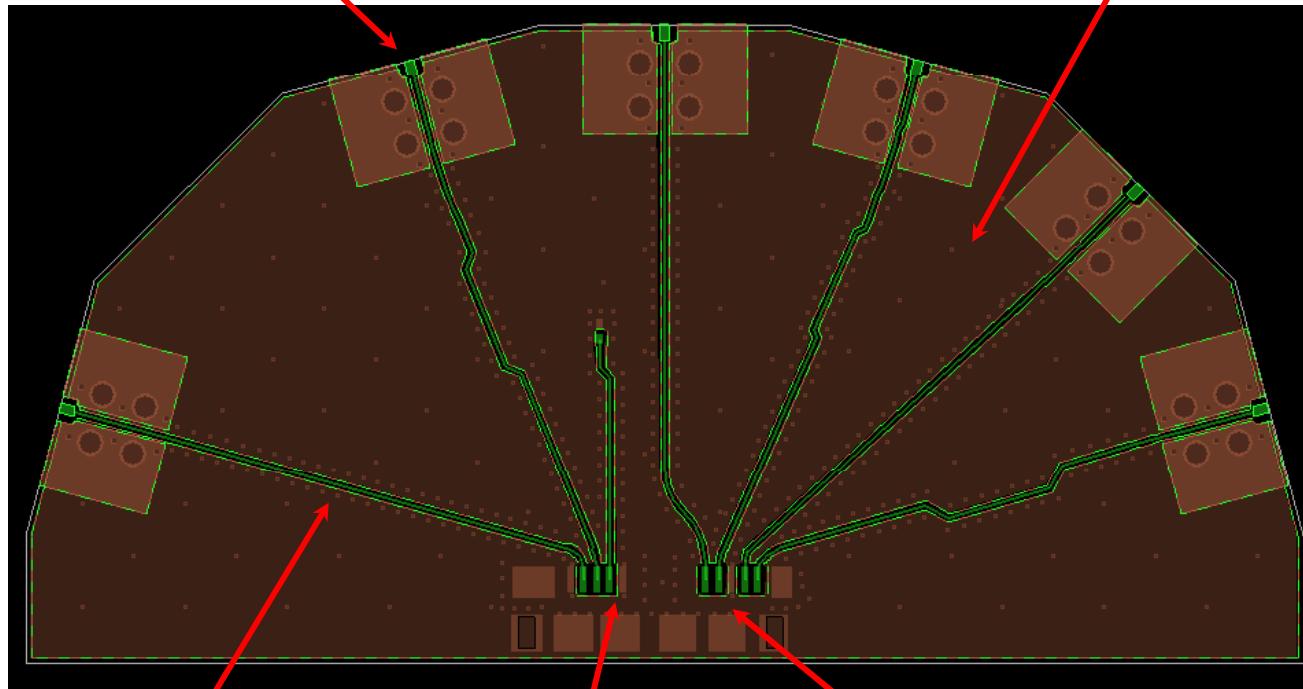
- To accommodate thicker cables, SMAs that are placed side by side should have a pitch  $>0.5''$  (0.75'' recommended).



# Hirose micro-B test board layout

*Optimized SMA footprint*

*Stitching vias in ground plane*



*Coplanar traces*

*Ground vias near ground pins*

*Terminate unused pins*

# PCB stack up

Layer	Cu Thick. (mils)	Cu Foil wt (oz)	DK	Lam. Thick. (mils)	Description
1	2.00	0.5 oz	3.80	3.75	Foil, 0.5 oz Prepreg FR408 2113(57) 18x24G
2	0.60	0.5 oz	4.00	18.00	Core FR408 18mils 2-7 628 1-2116 0.5 oz / 0.5 oz 18x24G
			3.80	10.20	Prepreg FR408 2116(55)/2116(55) 18x24G
			4.00	18.00	Core FR408 18mils 2-7 628 1-2116 0.5 oz / 0.5 oz 18x24G
3	0.60	0.5 oz			
4	2.00	0.5 oz	3.80	3.75	Prepreg FR408 2113(57) 18x24G Foil, 0.5 oz

Layers	Drill Type	Via Fill	54.90	Thickness over Laminate
1 - 4	PTH	--	58.90	Thickness over Copper
			60.30	Thickness over Soldermask

Layer	Structure Type	Coated Microstrip	Target Impedance (ohms)	Impedance Tolerance (ohms)	Target Linewidth (mils)	Edge Coupled Pitch * (mils)	Reference Layers	Modelled Linewidth (mils)	Modelled Impedance (ohms)	CoPlaner Space (mils)
1	Single Ended	No	50.00	+/-5	6.00	0.00	(2)	6.50	49.43	5

## Summary

- Suggestions for ways to optimize the USB 3 connector test board were presented.
- Hirose's USB 3 micro-B receptacle test board was presented incorporating the mentioned recommendations.



***Thank you !***

**<http://www.hiroseusa.com>**

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