

Section 5 PWB Design

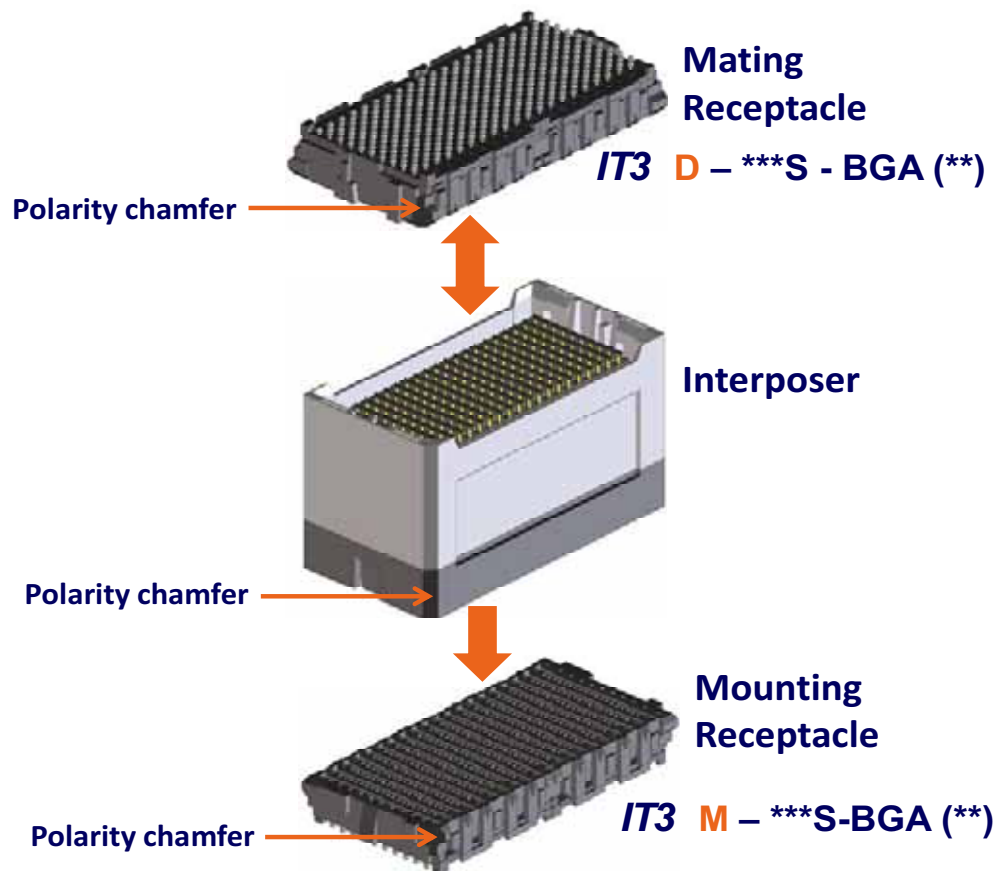
The Hirose IT3 connector's footprint is a staggered area array that allows space for easy via placement and signal routing between pads. Each row of I/O's alternates signal and ground interconnections. It is mounted to the board as a lightweight receptacle, and an interposer is used to connect to parallel PWBs at multiple different height options. Spacers must be used in conjunction with the interposers to help reinforce the structure of the final multi-PWB assembly.

This section of the Design Note discusses multi-connector systems, clearance between connectors, interposer direction, and alignment tolerances.

5.1 Footprint

5.1.1 Polarity

Each receptacle and interposer has **one corner chamfered** to insure proper orientation during assembly and installation. The corner with the **chamfer is nearest to pin A1**.

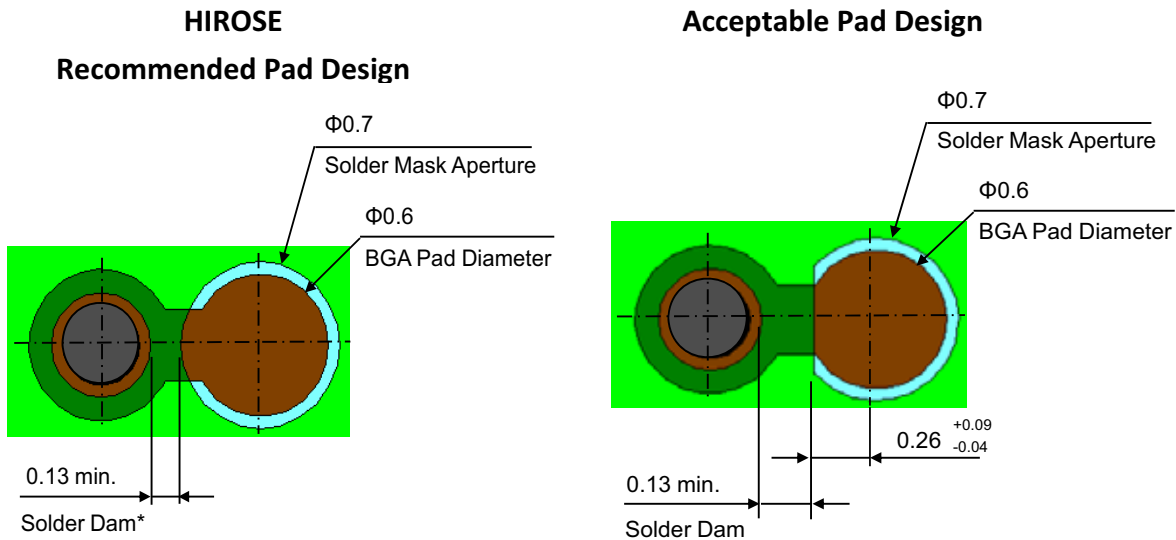


Annotation

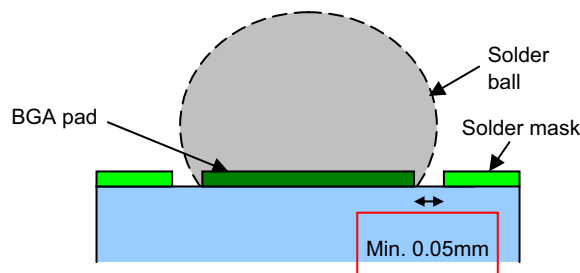
For **visual inspection** purposes, “**Pin 1**” should be denoted on the silkscreen of the PWB by a **specific marking** (e.g. asterisk or other accepted symbol) near the A1 contact location and chamfer.

5.1.2 Pad Specification

0.6mm diameter Non-Solder Mask Defined (NSMD), also known as *copper defined* or *metal defined*, pads are recommended. Recommended sizes and clearances are shown below:



* All dimensions shown are in mm



Cross Section of Pad and Solder ball

- Keep minimum clearance 0.05mm between BGA pad and solder mask to achieve “copper defined BGA pad”.
- BGA pad finish: OSP (Organic Solderability Preservative) or HASL (Hot Air Solder Leveler).
- The drill diameter of 0.34mm is for reference only. Use the proper aspect ratio of board thickness to via drill diameter for each PCB fabricator.

Through-via sizes will depend on **PWB thickness** and fabricator's capabilities. Vias should be placed far enough from the pad to ensure a **minimum solder dam width of 0.13mm**. **Circular openings** in the solder mask are **preferred**, but **D-shape openings** are **acceptable** if the minimum spacing requirement is met.

PWB pad finish is typically **Organic Solderability Preservative (OSP)** or **Hot Air Solder Level (HASL)**, but the component can also be used with Electroless Nickel-Immersion Gold (ENIG), Immersion Silver and Immersion Tin.

The **stencil apertures** should be **0.54mm circles**, concentric with the copper pads. This represents a 10% reduction from the diameter of the pad to compensate for typical variations in the assembly process.

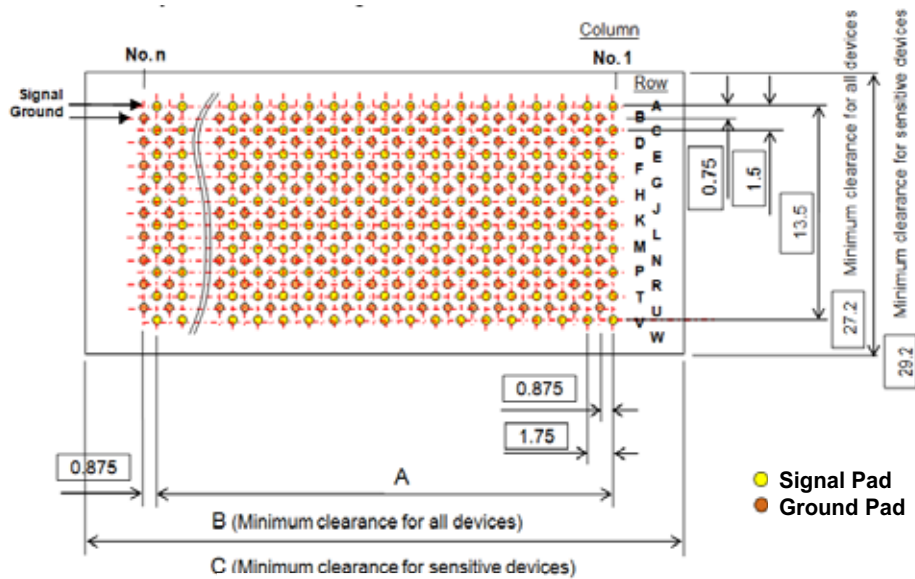
The specified clearance, or **solder mask relief**, from the copper feature is **0.05mm**.

Precaution

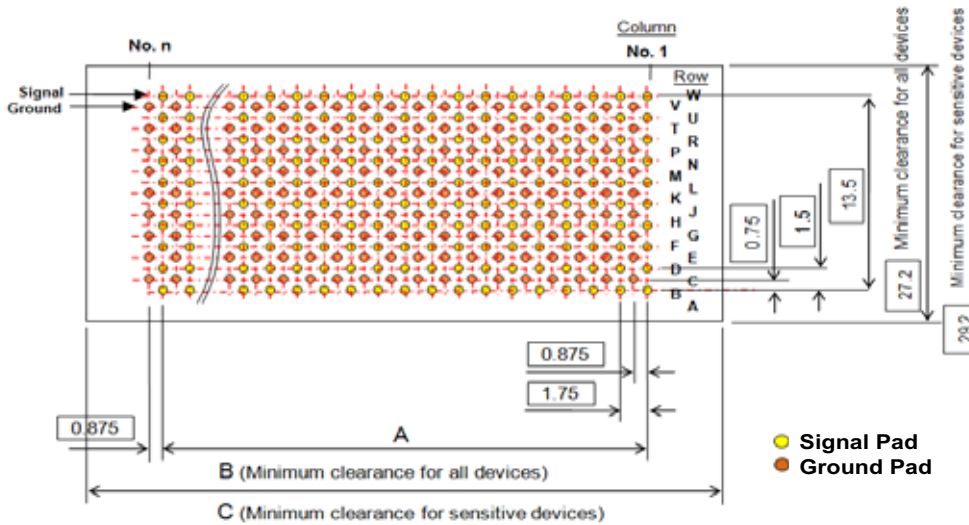
Verify fabricator capability. **Solder mask registration** must be accurate to at least **0.05mm**. PWB fabricator's registration capability should be verified. Depending on the thickness of PWB, fabricator's **aspect ratio** capabilities **for through vias** should also be verified.



5.1.3 Component Footprint and Contact Assignment



Mounting Receptacle – IT3-M



Mating Receptacle – IT3-D

* All dimensions shown are in mm.

Dimension (mm)	100	200	300
A	15.75	33.25	50.75
B	28.10	45.60	63.10
C	30.10	47.50	65.10

5.1.4 Contact Assignment

Figure 1 shows the side view of the IT3 connector. Figures 2 and 3 show the pin assignments on the PCB. Odd-numbered columns are signals and the even-numbered columns are grounds.

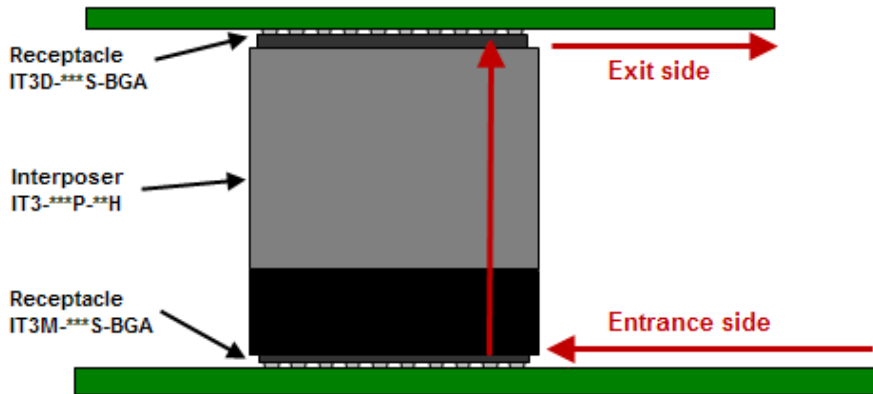


Figure 1 IT3 connector side view

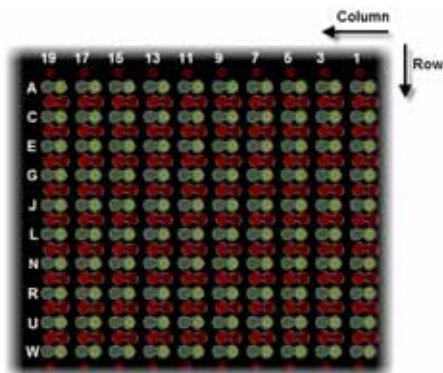


Figure 2 BGA pin-out on Motherboard PCB

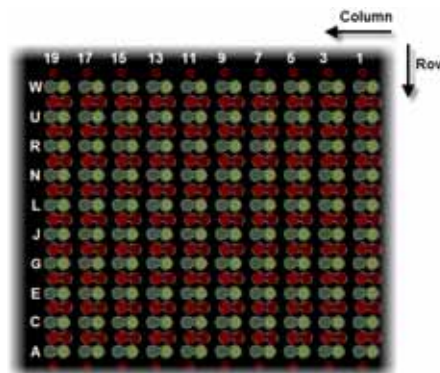


Figure 3 BGA pin-out on Daughterboard PCB

5.1.5 Routing Suggestions / Examples

The traces are routed in the column direction, avoiding going over the anti-pad. To avoid intra-pair skews, the trace lengths are matched. All trace bends are at 45-degree angles. Routing on adjacent dual strip line layers is not recommended and non-functional signal pads should be removed. Figures 4, 5 and 6 show examples of BGA pad layout, single-ended trace and differential trace routing on the PCB.

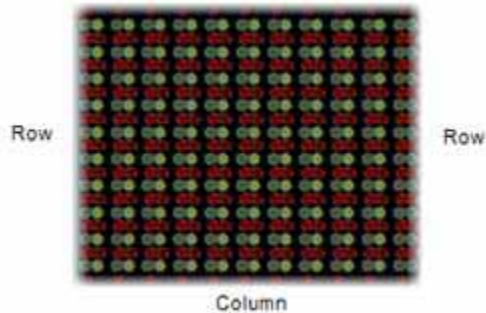


Figure 4 BGA Pad Layout on PCB

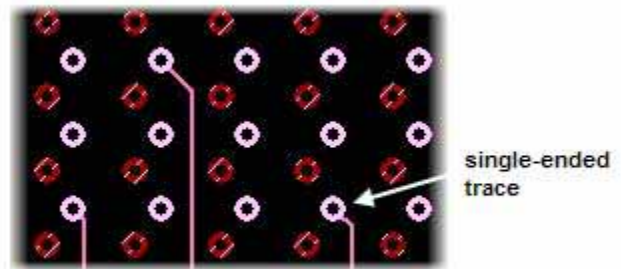


Figure 5 BGA Pad Layout on PCB

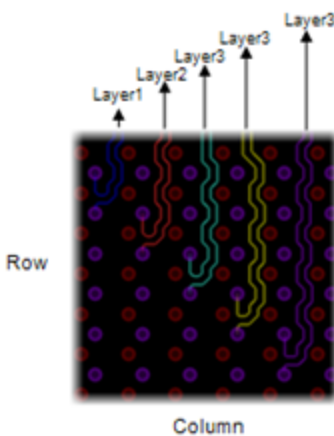


Figure 6-a Differential Routing

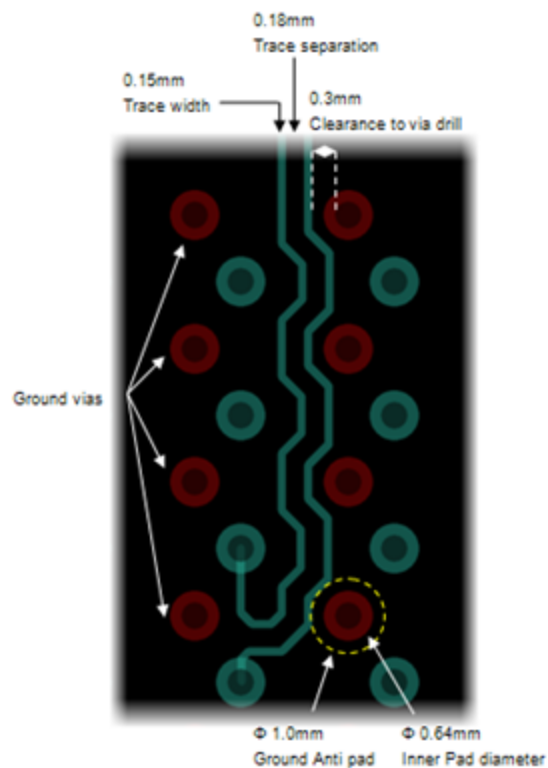


Figure 6-b Details of differential routing design

As shown in Figure 7, a minimum of three routing layers must be used on the PCB. Also, additional columns and rows of ground vias are added beyond row A, row W, and column 19 (for 100 pos.) to ensure that each signal via on the PCB is surrounded by four ground vias.

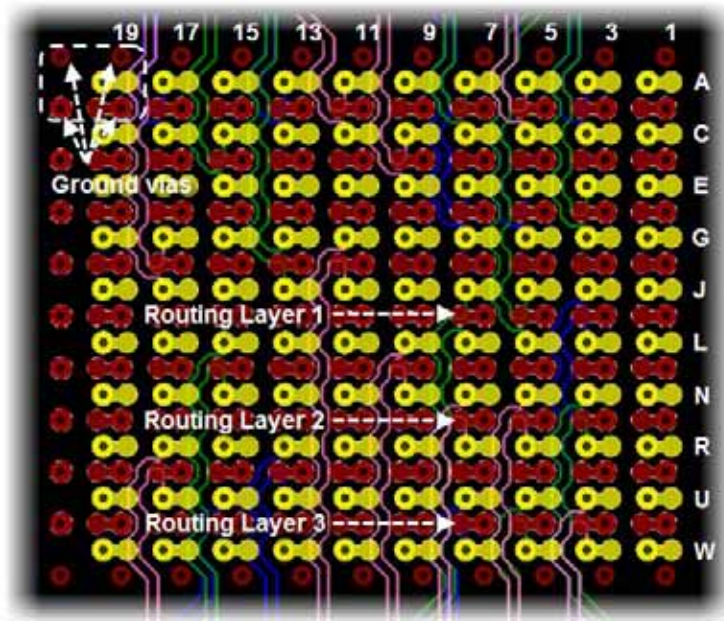


Figure 7 IT5 connector pin-out

A suggested trace routing example for differential signals is shown in Figure 11, with the stack up from Figure 12. The width and spacing of the differential signal traces must satisfy the following criteria:

$$2 * W + S < CP - D - 2 * C_{dt}$$

$$2 * W + S < CP - W_a$$

$$2 * W + S < C_{g1} - \frac{D_g}{2} - C_{gdt} - \frac{D}{2} - C_{dt}$$

$$2 * W + S < C_{g1} - \frac{W_a}{2} - \frac{W_{ag}}{2}$$

For a 120 mil board, the signal and ground via sizes, and clearance from via drill are fixed. Therefore, only the trace width and spacing are adjustable.

Single ended traces can be routed anywhere within the limits of the total routing width (TRW) for the differential signals.

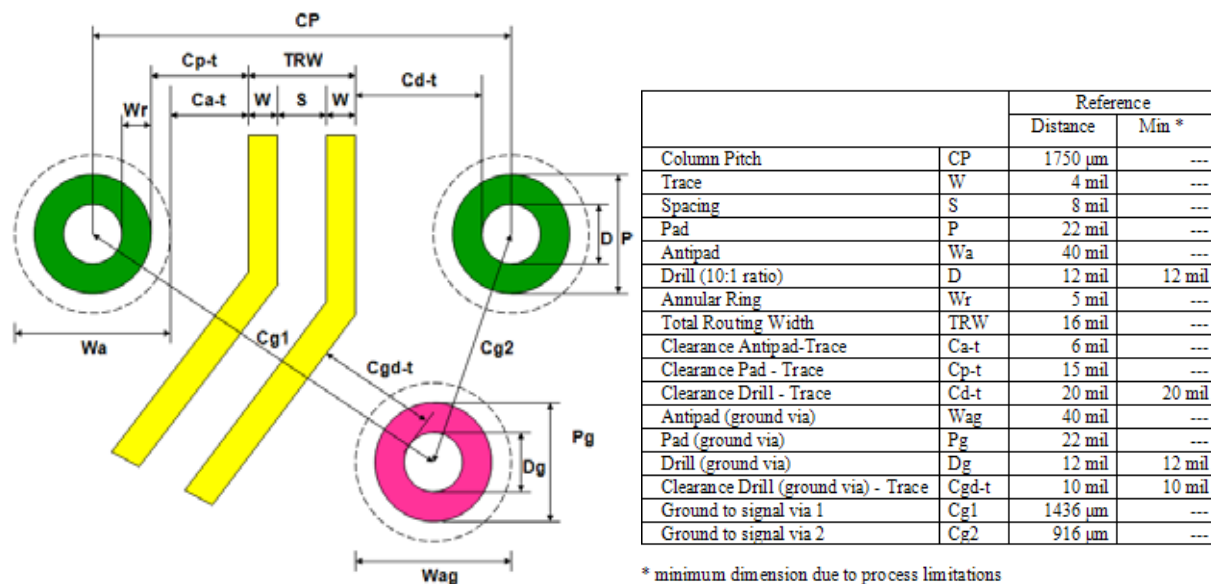


Figure 11 Trace routing example

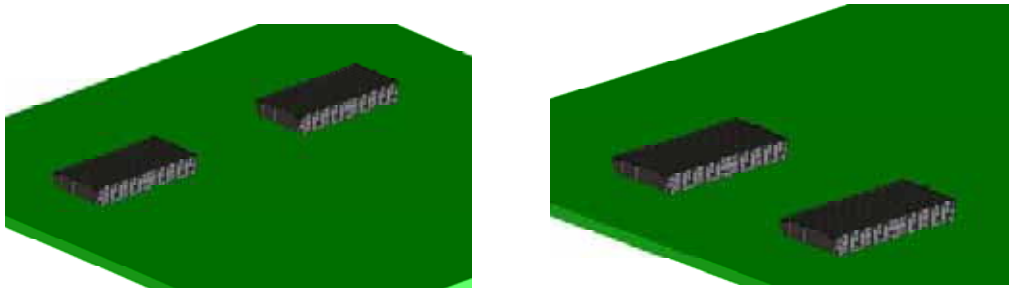
Layer No.			Mil
		Solder mask	0.5
1	TOP		2.84
		Pre-preg	4.5
2	Ground		0.7
		Core	3
3	Sig 1		0.7
		Pre-preg	3.5
4	Sig 2		0.7
		Core	3
5	Ground		0.7
		Pre-preg	3.5
6	Ground		0.7
		Core	3
7	Sig 3		0.7
		Pre-preg	3.5
8	Sig 4		0.7
		Core	3
9	Ground		0.7
		Pre-preg	3.5
10	Ground		0.7
		Core	3
11	Sig 5		0.7
		Pre-preg	3.5
12	Sig 6		0.7
		Core	3
13	Ground		0.7
		Pre-preg	3.5
14	Ground		0.7
		Core	3
15	Sig 7		0.7
		Pre-preg	3.5
16	Sig 8		0.7
		Core	3
17	Ground		0.7
		Pre-preg	3.5
18	Ground		0.7
		Core	3
19	Sig 9		0.7
		Pre-preg	3.5
20	Sig10		0.7
		Core	3
21	Ground		0.7
		Pre-preg	3.5
22	Ground		0.7
		Core	3
23	Sig11		0.7
		Pre-preg	3.5
24	Sig12		0.7
		Core	3
25	Ground		0.7
		Pre-preg	3.5
26	Ground		0.7
		Core	3
27	Sig13		0.7
		Pre-preg	3.5
28	Sig14		0.7
		Core	3
29	Ground		0.7
		Pre-preg	4.5
30	BOTTOM		2.84
		Solder mask	0.5
	Total thickness (mil)		121.78

Figure 12 PCB stack up example

5.2 Multi-Connector Systems

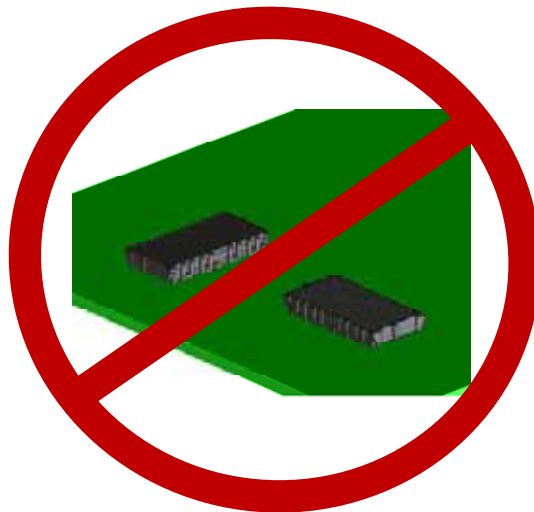
The **IT3** connectors can be used singularly or in combination with other **IT3** connectors.

If multiple connectors are used on the same PWB, they must be oriented in the same direction, as shown below:



Correct Orientations

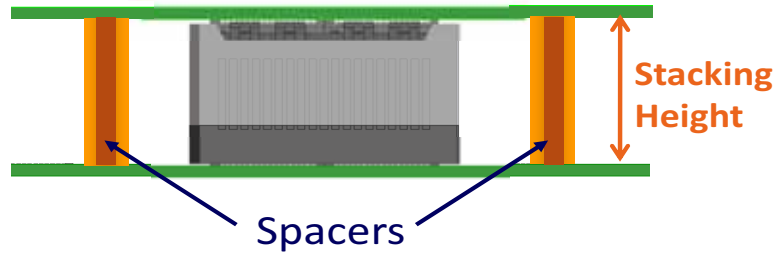
It is not recommended to mix orientations:



Do not mix orientations

5.3 Spacers

Spacers are required to support the PWB's and protect the BGA solder joints.



Suggested spacer style is shown below:

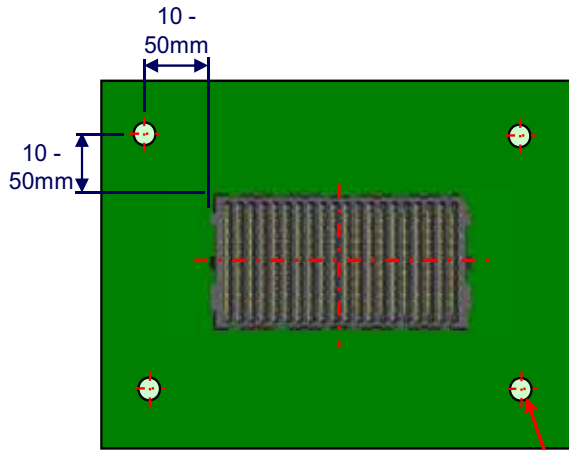


Spacer, male-male, M3 thread

The recommended spacer height corresponds to the interposer stacking height as shown in the chart below:

Stacking Height	Recommended Spacer Height
17 mm	17 +/-0.127 mm
20 mm	20 +/-0.127 mm
22 mm	22 +/-0.127 mm
25 mm	25 +/-0.127 mm
26 mm	26 +/-0.127 mm
28 mm	28 +/-0.127 mm
30 mm	30 +/-0.127 mm
32 mm	32 +/-0.127 mm
38 mm	38 +/-0.127 mm
40 mm	40 +/-0.127 mm

5.3.1 Spacer Location



Two spacers located diagonally are minimally required. Some applications may require four spacers.

Spacers should be located 10 – 50 mm from the corners of the receptacles to prevent excessive mechanical loading on the interconnections.

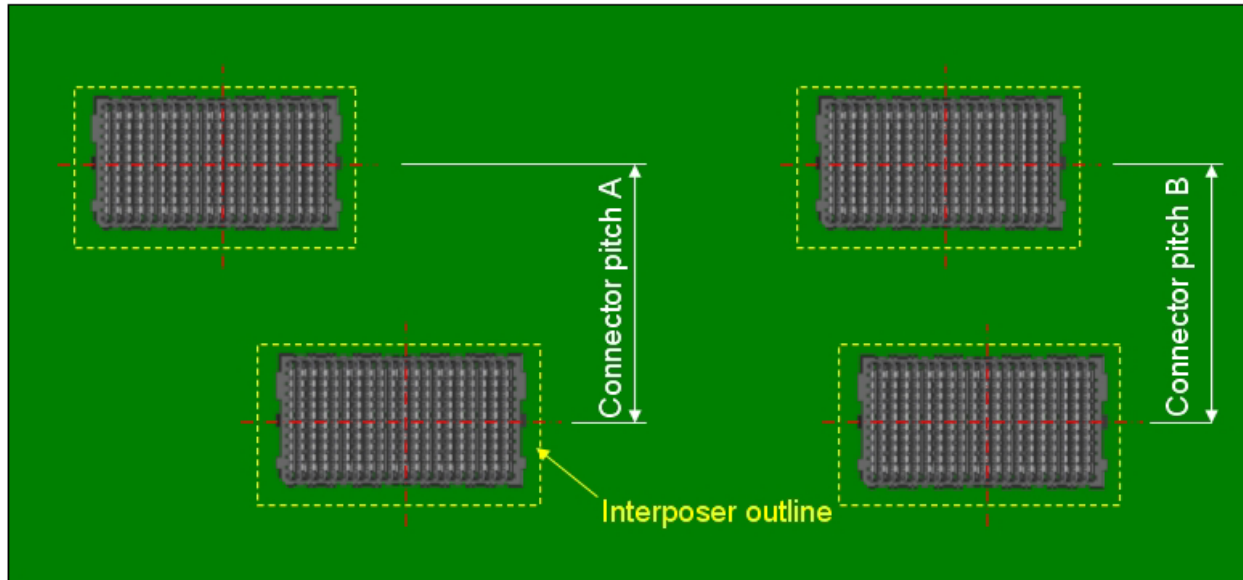
If assembly will be subjected to vibration, spacers should be located to prevent resonance, and additional spacers may be required.

$\Phi 3.5$
Non plated through hole

Recommended Spacer Location

5.4 Clearance between Connectors and Other Components and PCB Edge

Parallel Mounting



Not in scale

(A) If **overlap distance is less than half** the length of the connector:

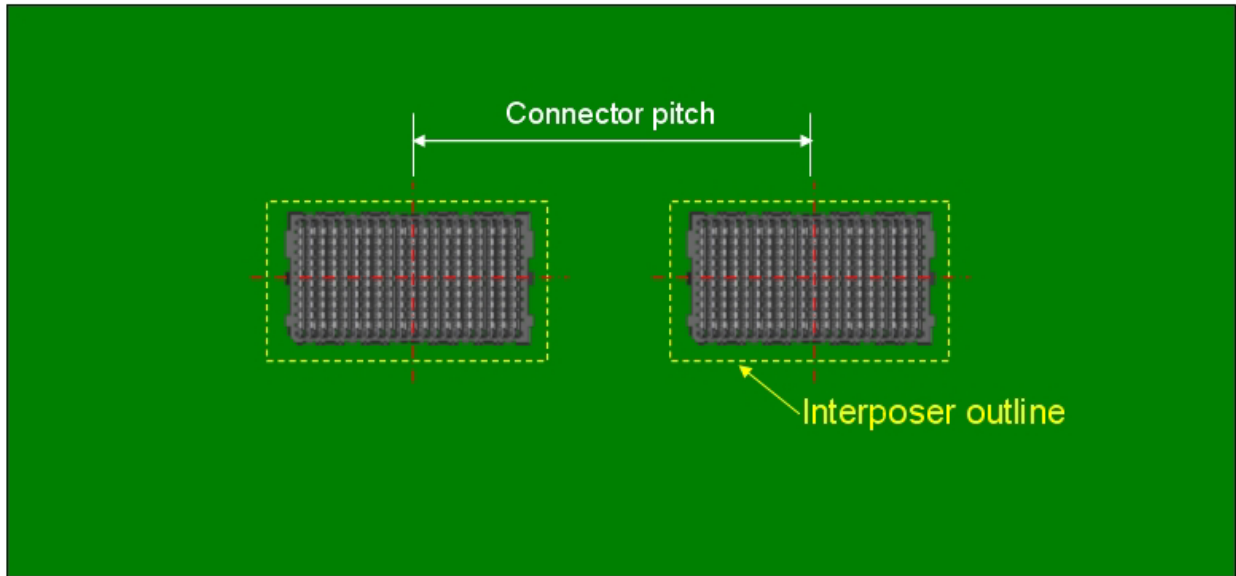
Socket Combinations	Connector Pitch A (Max)	Connector Pitch A (Min)
All combinations	24.10 mm	209.20 mm

(B) If **overlap distance is more than half** the length of the connector:

Socket Combinations	Connector Pitch B (Max)	Connector Pitch B (Min)
All combinations	31.00	209.20

Suggested clearances are based on accessibility to grip interposer for purposes of disassembly and field replacement.

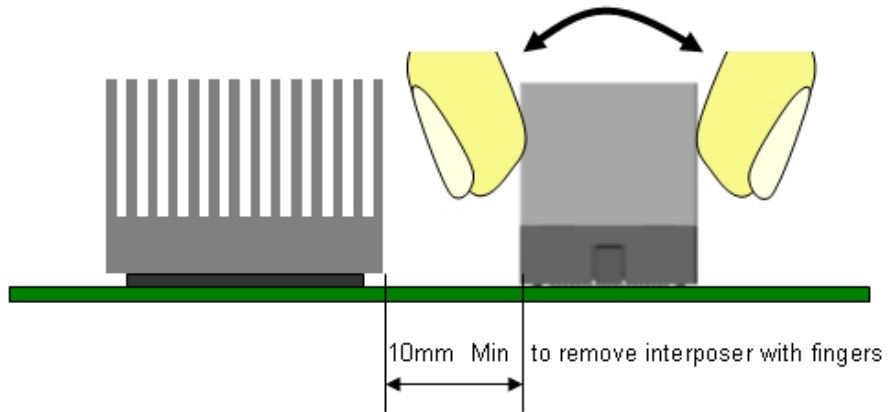
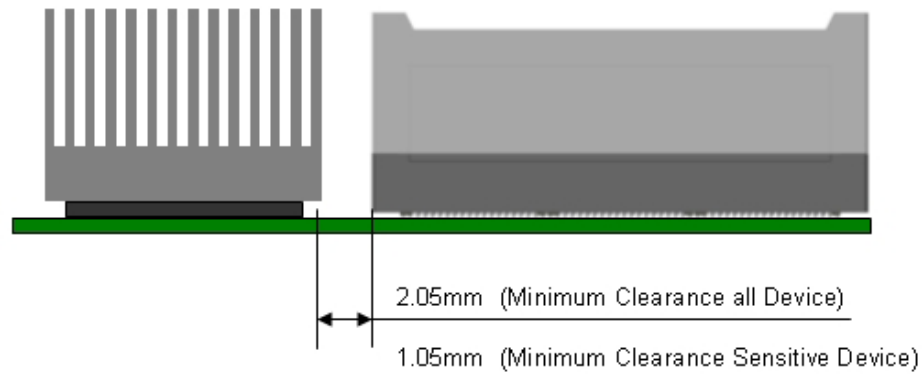
Tandem Mounting



Not in scale

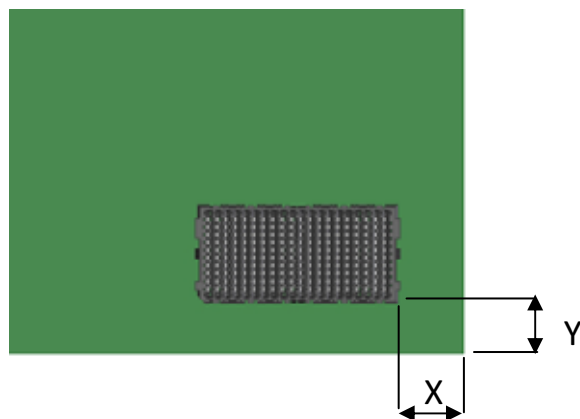
Socket Combinations	Connector Minimum Pitch (mm)	Connector Maximum Pitch (mm)
IT3-100pos + IT3-100pos	26.05	211.00
IT3-100pos + IT3-200 pos	34.80	219.75
IT3-100pos + IT3-300 pos	43.55	228.50
IT3-200pos + IT3-200 pos	43.55	228.50
IT3-200pos + IT3-300 pos	52.30	237.25
IT3-300pos + IT3-300 pos	61.05	246.00

Clearances between a connector and other components



Clearance between the receptacle and PCB edges

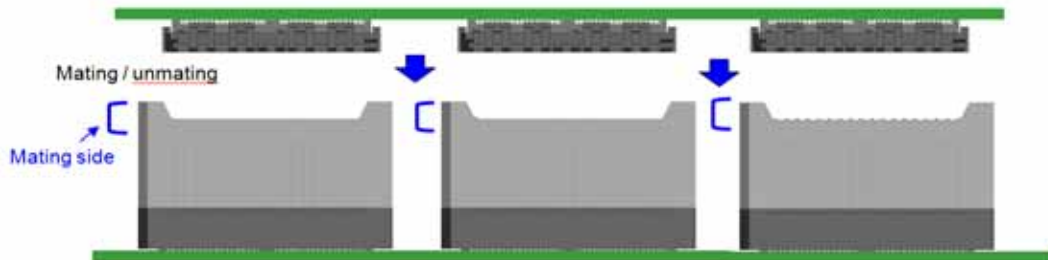
Please communicate CEM regarding the clearance especially when requiring the top side reflow.



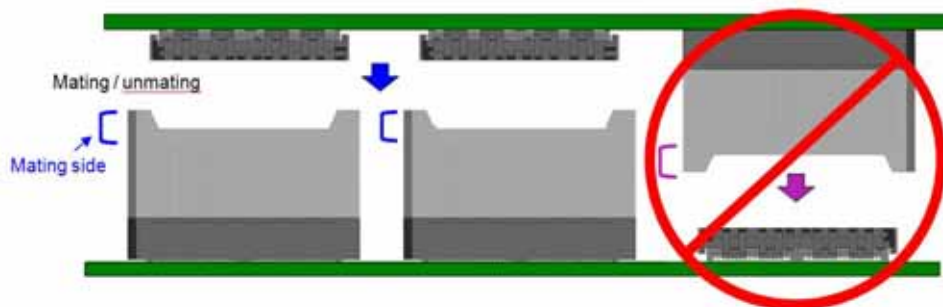
5.5 Interposer Direction

Do not mix mating and mounting receptacles on the same PWB.

All interposers must engage in the same direction, as shown below:



Correct Method – all connectors mate in same direction

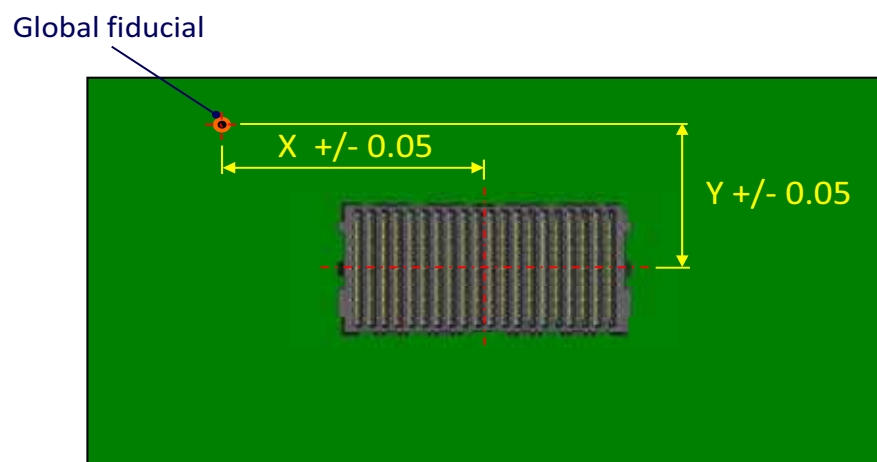


Incorrect Method – connectors mate in different directions

5.6 Alignment Tolerances

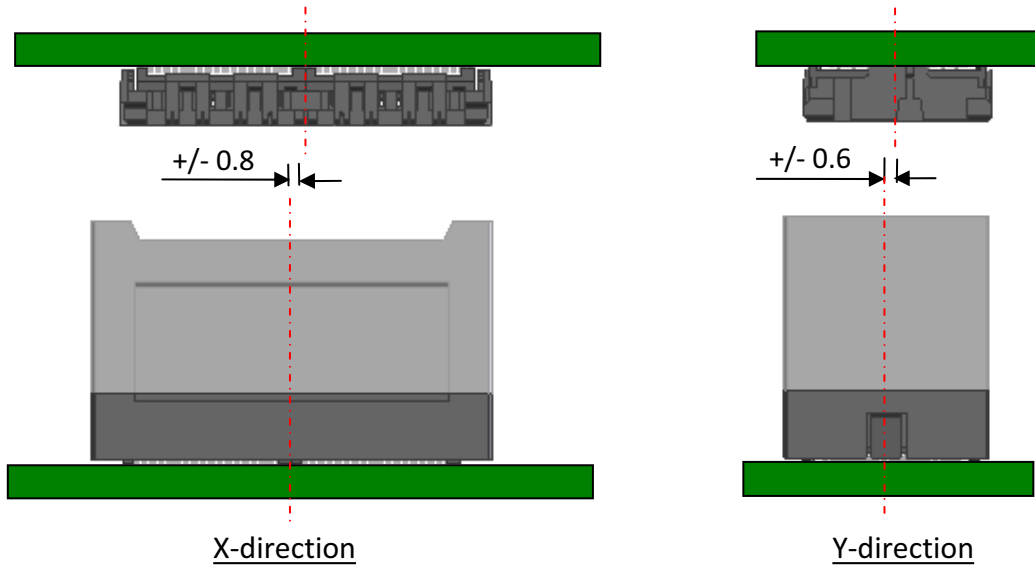
5.6.1 Mounting Tolerances

Mounting tolerances of $\pm 0.05\text{mm}$ are required for robust SMT assembly and to ensure proper mating fits in cases of multiple connectors:



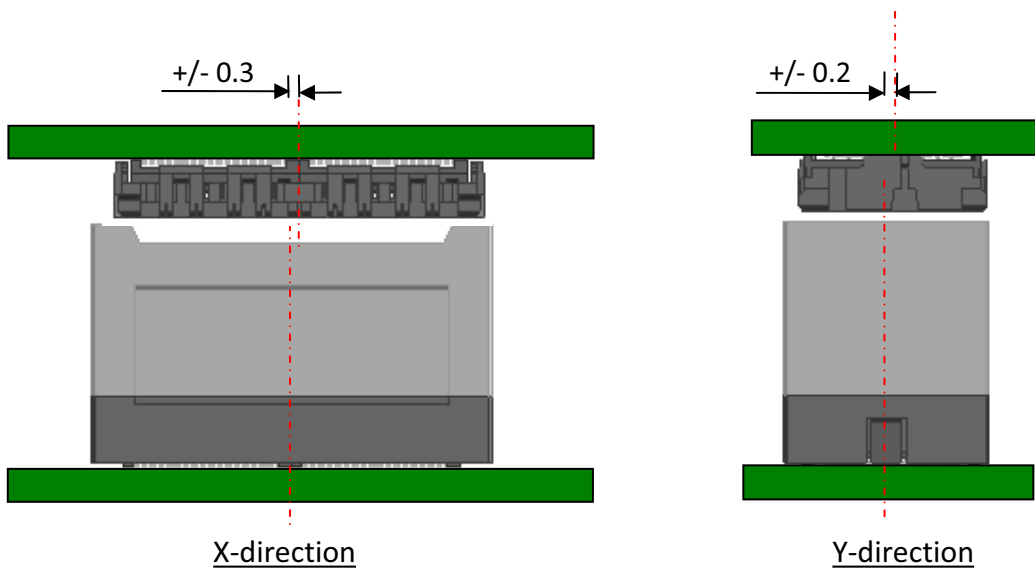
*All dimensions shown are in mm.

5.6.2 Mating Self Alignment



5.6.3 Mating Tolerances

Due to its 3-piece design, the IT3 connector system can accept mating tolerances of up to ± 0.3 mm tolerance in the X-axis and up to ± 0.2 mm in the Y-axis.



* All dimensions shown are in mm